10-bit to 130 MSPS low-power high-speed ADC

SPECIFICATION

1 FEATURES

- TSMC CMOS LP 65 nm
- Resolution 10 bit
- Different power supplies for digital (1.2 V) and analog parts (1.2 V)
- Sampling rate up to 130 MSPS
- Standby mode (current consumption 10 uA)
- Low-power dissipation:
  34 mW at 130 MSPS
  25 mW at 80 MSPS
  21 mW at 50 MSPS
- Differential input voltage range 1.2 V peak-to-peak
- Full power bandwidth:
  260 MHz at 130 MSPS
  160 MHz at 80 MSPS
  100 MHz at 50 MSPS
- Spurious-free dynamic range:
  68 dB at 130 MSPS and fin = 8.125 MHz
  69 dB at 80 MSPS and fin = 5 MHz
  69 dB at 50 MSPS and fin = 3.125 MHz
- Signal-to-noise ratio:
  60 dB at 130 MSPS and fin = 8.125 MHz
  60 dB at 80 MSPS and fin = 5 MHz
  60 dB at 50 MSPS and fin = 3.125 MHz
- Differential nonlinearity 0.5 LSB
- Integral nonlinearity 1 LSB
- Small area
- Portable to other technologies (upon request)

2 APPLICATION

- WiFi, WiMax
- Mobile Communications
- High quality imaging video systems
- Data acquisition systems
- Portable ultrasound and digital beam-forming systems

3 OVERVIEW

The 10-bit to 130 MSPS low-power high-speed ADC is based on pipelined architecture. ADC contains a five main blocks: sample and hold, core ADC, digital error correction, timing generation, reference voltage. ADC requires: 1.08÷1.32 V analog supply, 1.08÷1.32 V digital supply; reference current 4.95÷5.05 uA; differential reference voltage 1.08÷1.32 V and 0 V; differential input clock with duty cycle 45÷55 %. ADC supports standby mode. There is also the ability to configure the operating modes of the ADC with digital registers: register en_d<1:0> controls the differential input clock, register cr<11:0> controls the modes of the core ADC, register adj_sh<3:0> adjusts current of the sample and hold, register adj_md<3:0> adjusts current of the core ADC.
The block is designed on TSMC CMOS 65 nm technology.

4 STRUCTURE

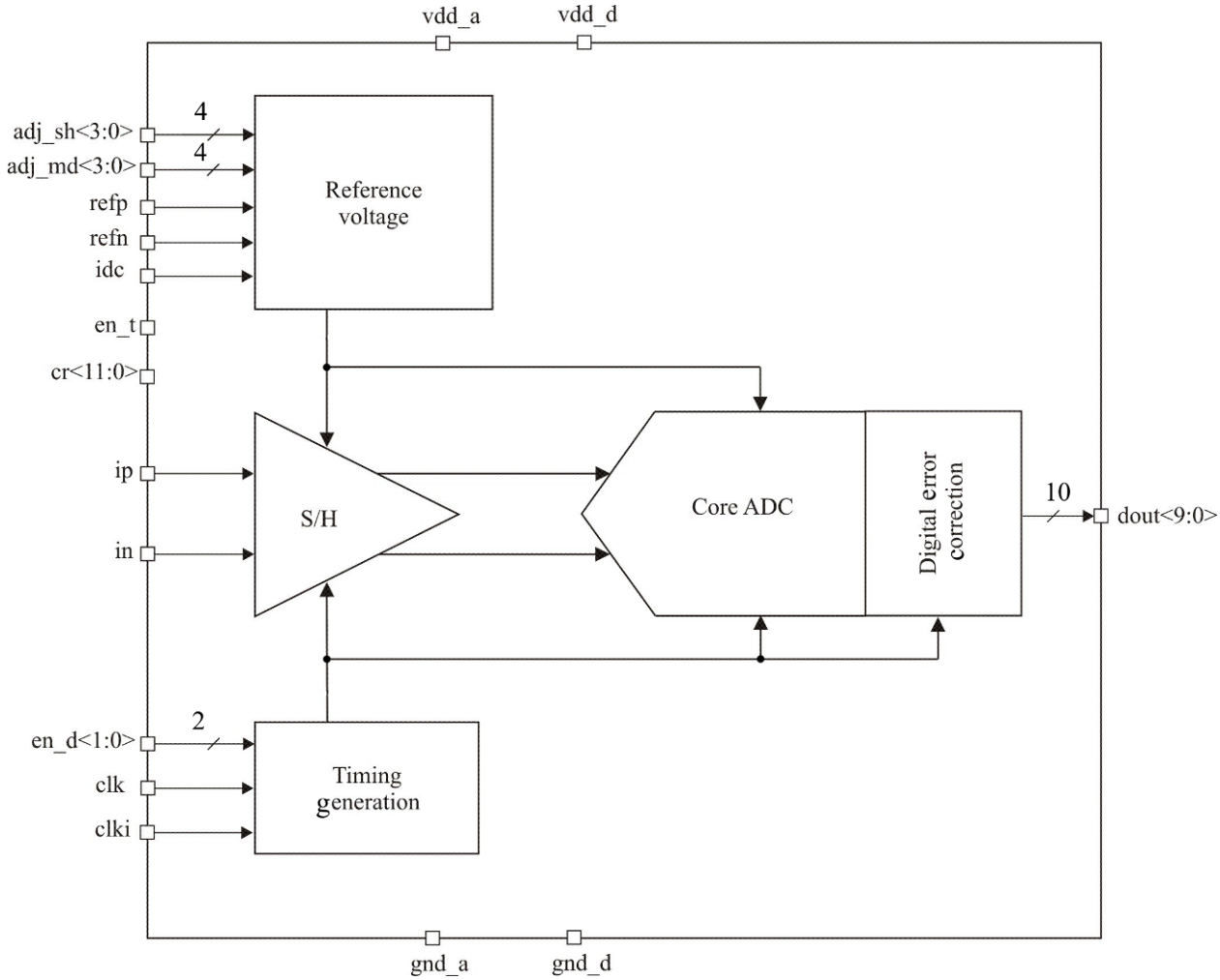

Figure 1: Low-power high-speed 10-bit ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
idc	I	Reference current (5 uA)
ip	I	Analog differential input
in		
clk	I	Differential input clock
clki	I	
refp	I	Differential reference voltage
refn	I	
en_t	I	Enable total
en_d<1:0>	I	Register of control the differential input clock
cr<11:0>	I	Register of control modes the core ADC
adj_sh<3:0>	I	Register of adjust current the sample and hold
adj_md<3:0>	I	Register of adjust current the core ADC
dout<9:0>	O	Output data
vdd_a	I/O	Analog block supply voltage
vdd_d	I/O	Digital blocks supply voltage
gnd_a	I/O	Analog blocks ground (1.2 V)
gnd_d	I/O	Digital blocks ground (1.2 V)

6 LAYOUT DESRIPTION

Low-power high-speed ADC layout dimensions are given in the table 1.

Table 1: Block dimension

Dimension	Value	Unit
Height	480	um
Width	592	um

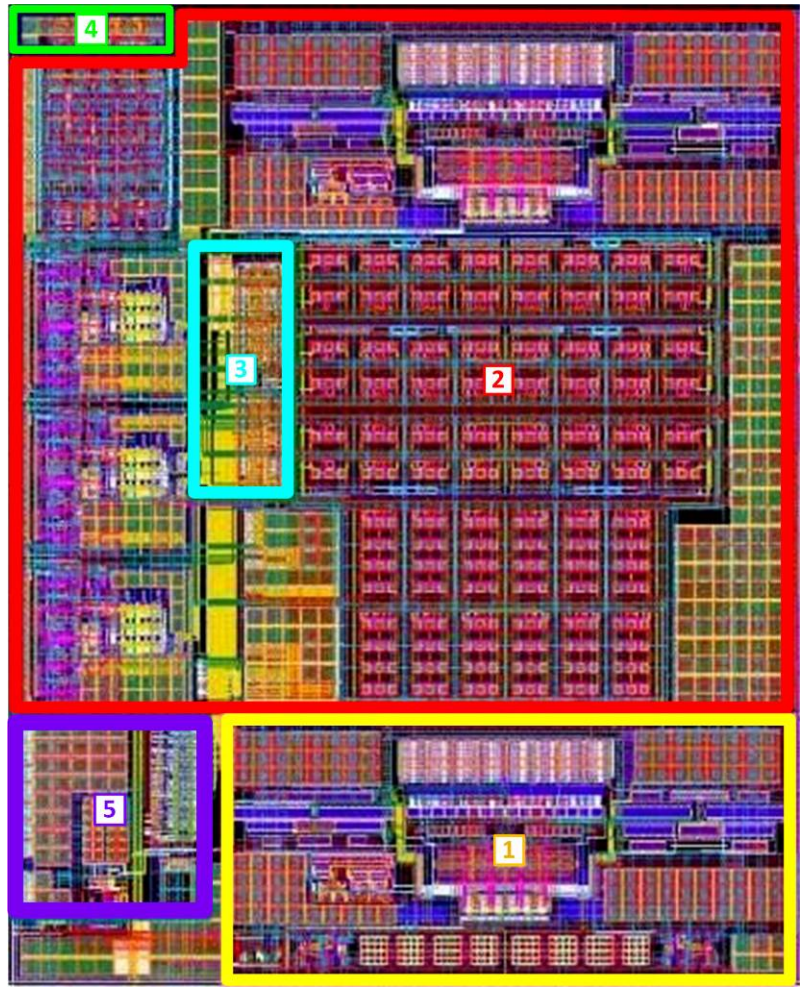

Figure 2: Layout low-power high-speed ADC

1. Sample and hold
2. ADC core
3. Reference voltage
4. Digital error correction
5. Timing generator

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS LP 65nm
Status silicon proven
Area 0.28 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd_a}= 1.08÷1.32 V, V_{dd_d}= 1.08÷1.32 V and T_j =-40÷+125°C, typical values are at V_{dd_a} = 1.2 V, V_{dd_d}= 1.2 V, T_j = +27°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Operating temperature range	T_j	-	-40	27	+125	°C
Analog blocks supply voltage	V_{dd_a}	-	1.08	1.2	1.32	V
Digital blocks supply voltage	V_{dd_d}	-	1.08	1.2	1.32	V
Differential reference voltage	V_{refp}	-	1.08	1.2	1.32	V
	V_{refn}	-	-	0	-	V
Reference current	I_{ref}	-	4.95	5	5.05	uA
Duty cycle	S	-	45	50	55	%
Resolution	N	-	-	10	-	bit
Sampling rate	F_s	-	-	-	130	MSPS
Power dissipation	P_{cn}	F_s= 130 MSPS adj_sh<3:0>=1010 adj_md<3:0>=1010	-	34	-	mW
		F_s = 80 MSPS adj_sh<3:0>=0111 adj_md<3:0>=0111	-	25	-	mW
		F_s = 50 MSPS adj_sh<3:0>=0110 adj_md<3:0>=0110	-	21	-	mW
Current consumption	I_{cn}	F_s = 130 MSPS adj_sh<3:0>=1010 adj_md<3:0>=1010	-	28	-	mA
		F_s = 80 MSPS adj_sh<3:0>=0111 adj_md<3:0>=0111	-	20	-	mA
		F_s = 50 MSPS adj_sh<3:0>=0110 adj_md<3:0>=0110	-	17	-	mA
Standby current	I_s	-	-	10	-	uA
Differential input voltage range peak-to-peak	$A_{IN\ p\text{-}p}$	-	-	1.2	-	V
Input common mode voltage	U	-	-	0.6	-	V
Full power bandwidth	F_B	F_s = 130 MSPS	-	260	-	MHz
		F_s = 80 MSPS	-	160	-	MHz
		F_s = 50 MSPS	-	100	-	MHz

Table “Electrical characteristics” (continue)

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Spurious-free dynamic range	SFDR	F_s = 130 MSPS, fin = 8.125 MHz	-	68	-	dB
		F_s = 80 MSPS, fin = 5 MHz	-	69	-	dB
		F_s = 50 MSPS, fin = 3.125 MHz	-	69	-	dB
Signal-to-noise ratio	SNR	F_s = 130 MSPS, fin = 8.125 MHz	-	60	-	dB
		F_s = 80 MSPS, fin = 5 MHz	-	60	-	dB
		F_s = 50 MSPS, fin = 3.125 MHz	-	60	-	dB
Signal-to-noise and distortion ratio	SINAD	F_s = 130 MSPS, fin = 8.125 MHz	-	59	-	dB
		F_s = 80 MSPS, fin = 5 MHz	-	59	-	dB
		F_s = 50 MSPS, fin = 3.125 MHz	-	60	-	dB
Effective number of bits	ENOB	F_s = 130 MSPS	-	9.1	-	bit
		F_s = 80 MSPS	-	9.3	-	bit
		F_s = 50 MSPS	-	9.3	-	bit
Differential nonlinearity	DNL	F_s = 80 MSPS	-	0.5	-	LSB
Integral nonlinearity	INL	F_s = 80 MSPS	-	1	-	LSB
Input high-logic level	V_{IH}	For digital inputs	0.7 V_{dd_d}	-	-	V
Input low-logic level	V_{IL}		-	-	0.3 V_{dd_d}	V

8 TYPICAL CHARACTERISTICS

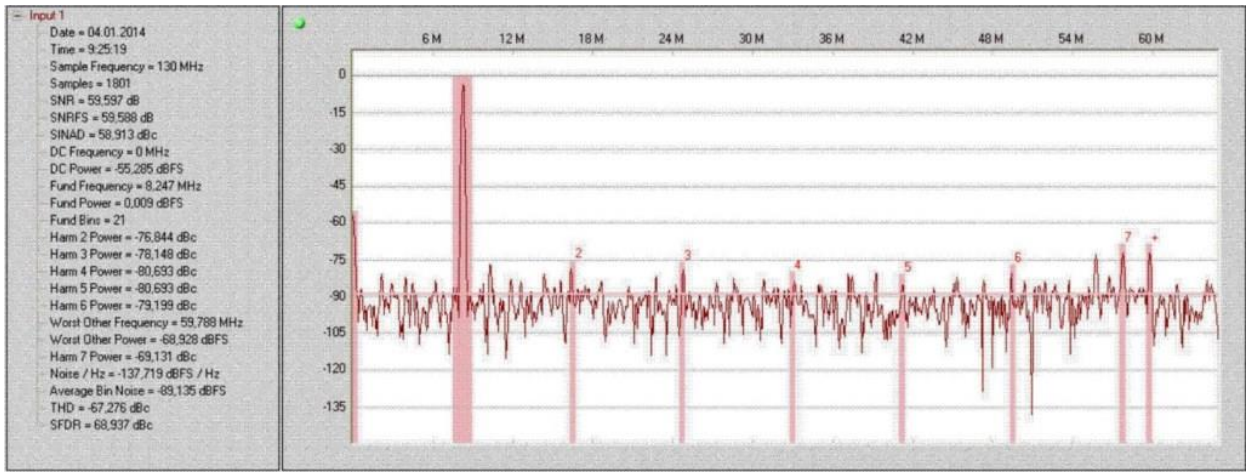

Figure 3: Spectrum, F_s= 130 MSPS

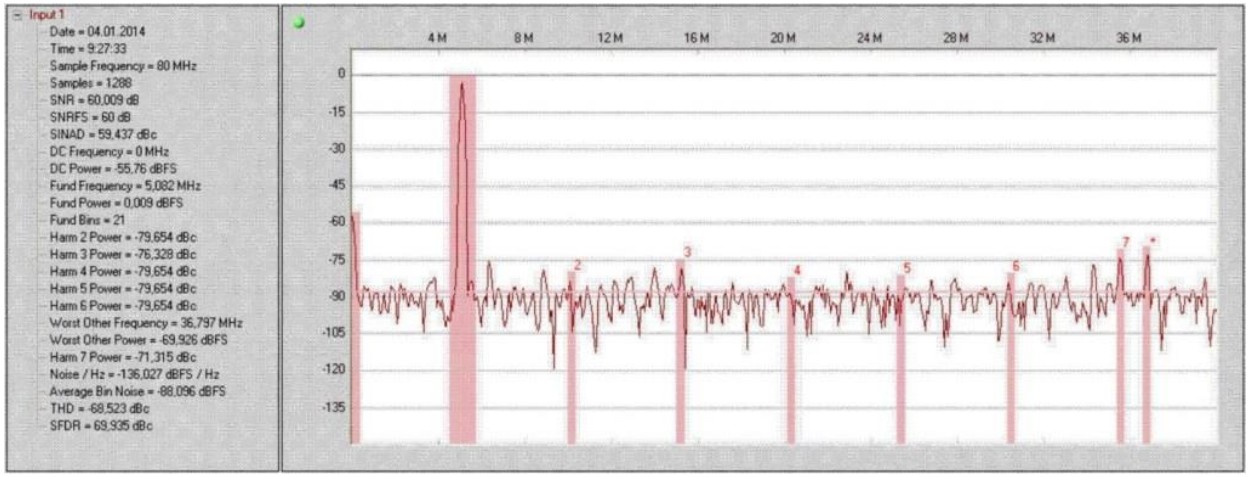

Figure 4: Spectrum, F_s = 80 MSPS

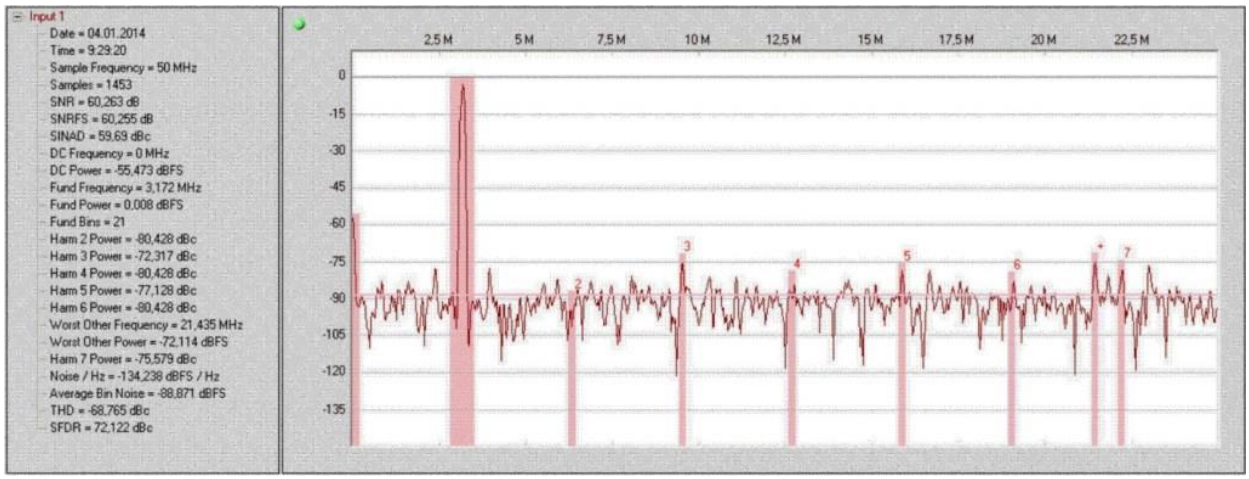

Figure 5: Spectrum, F_s = 50 MSPS

9 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Layout or blackbox
- Verilog, lef and lib files
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.1:

- Section 6 updated (refer to page 4)
- Subsection 7.1 updated (refer to page 5)
- Subsection 7.2 updated

From version 1.0:

- Section 1 updated (refer to page 1)