

12-bit 1-channel 4 MSPS ADC

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- Resolution 12 bit
- Single power supplies for digital and analog parts (2.5 V)
- Sampling rate up to 4 MSPS
- Standby mode (current consumption 50 nA)
- Low-power dissipation:
2.5 mW at 4 MSPS
- Differential full-scale input range peak-to-peak 2 V
- Dynamic performance:
70.2 dB SFDR, 57.2 dB SINAD at 1.5 MSPS and $f_{in}= 5$ MHz
69.0 dB SFDR, 56.0 dB SINAD at 2.5 MSPS and $f_{in}= 5$ MHz
69.5 dB SFDR, 52.4 dB SINAD at 4.0 MSPS and $f_{in}= 5$ MHz
- Compact die area 0.124 mm²
- Portable to other technologies (upon request)

2 APPLICATION

- WiFi, WiMax
- Mobile communications
- High quality imaging video systems
- Data acquisition systems
- Portable ultrasound and digital beam-forming systems

3 OVERVIEW

The 12-bit 4 MSPS ADC employs high-performance differential successive approximation architecture with sub-ranging and output offset compensation techniques. The ADC operates with sampling rate up to 4 MSPS and a corresponding input clock up to 52 MHz. The ADC supports standby mode and features low power consumption, compact area. The block is designed on TSMC CMOS 65 nm technology.

4 STRUCTURE

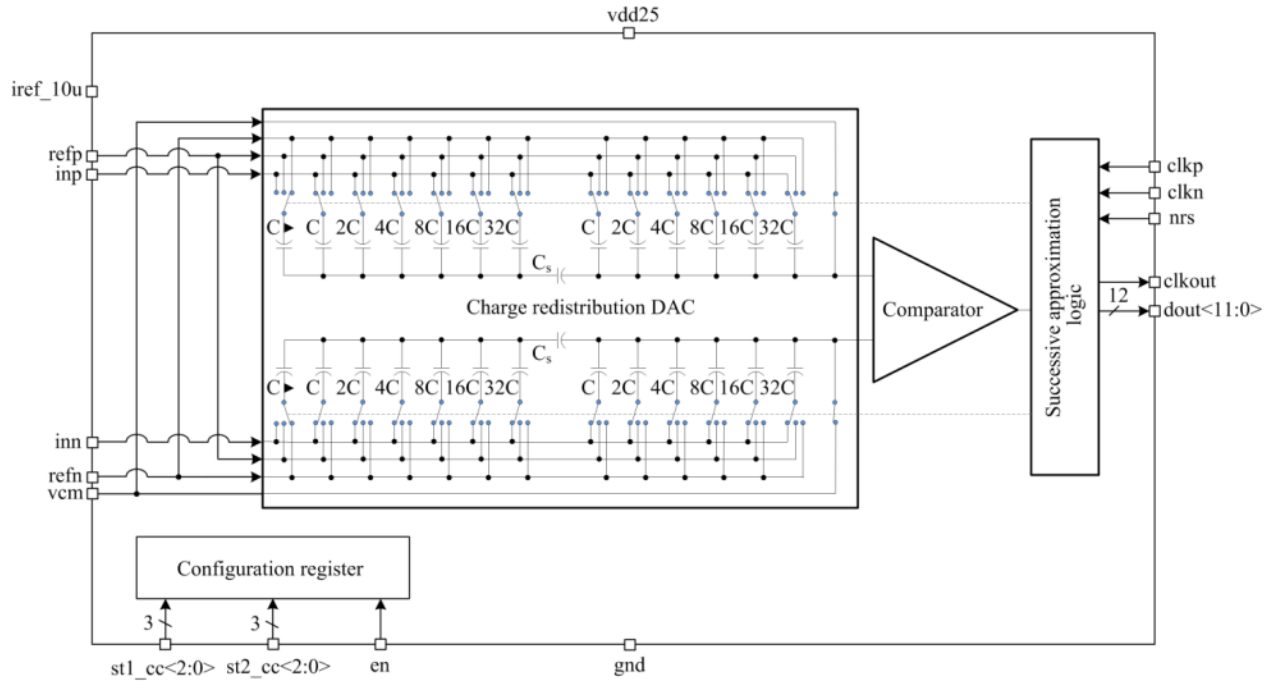


Figure 1: 12-bit 4MSPS ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
iref_10u	I	Reference current (10 uA)
inp	I	Analog differential input
inn		
en	I	ADC enable: “0” disabled “1” enabled
nrs	I	Reset signal: “0” enabled “1” disabled
clkp	I	52 MHz differential input clock
clkn		
refp	I	Positive reference voltage (1.75 V)
vcm	I	Common mode voltage (1.25 V)
refn	I	Negative reference voltage (0.75 V)
st1_cc<2:0>	I	Register of adjust current first pre-amplifier: “000” 0.25 mA ... with step of 0.25 mA “111” 2 mA
st2_cc<2:0>	I	Register of adjust current second pre-amplifier: “000” 0.25 mA ... with step of 0.25 mA “111” 2 mA
dout<11:0>	O	Output data
clkout	O	4 MHz output clock
vdd25	I/O	Supply voltage (2.5 V)
gnd	I/O	Ground

6 LAYOUT DESCRIPTION

ADC layout dimensions are given in the table 1.

Table 1: Block dimension

Dimension	Value	Unit
Height	163	um
Width	760	um

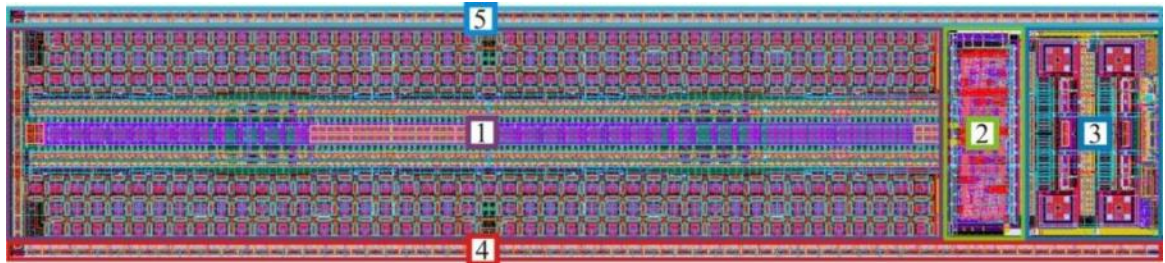


Figure 2: Layout 12-bit 4 MSPS ADC

1. Charge-redistribution DAC
2. Successive approximation logic
3. Comparator
4. Blocking capacitor
5. Blocking capacitor

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC CMOS 65nm
 Status _____ silicon proven
 Area _____ 0.124 mm²

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{dd25}=2.25\div 2.75$ V and $T_j=-40\div +85^\circ\text{C}$, typical values are at $V_{dd25}=2.5$ V, $T_j=27^\circ\text{C}$, single core, unless otherwise specified.

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
Operating temperature range	T_j	-	-40	27	+85	$^\circ\text{C}$
Power supply requirements						
Supply voltage	V_{dd25}	-	2.25	2.5	2.75	V
Analog current consumption	I_{ACN}	$F_S=1.5$ MSPS st1_cc<2:0> = "001" st2_cc<2:0> = "001"	-	0.75	-	mA
		$F_S=2.5$ MSPS st1_cc<2:0> = "001" st2_cc<2:0> = "001"	-	0.85	-	mA
		$F_S=4$ MSPS st1_cc<2:0> = "001" st2_cc<2:0> = "001"	-	1	-	mA
Current consumption in standby mode	I_S	-	-	50	-	nA
Total power consumption	P_{CN}	$F_S=1.5$ MSPS st1_cc<2:0> = "001" st2_cc<2:0> = "001"	-	1.9	-	mW
		$F_S=2.5$ MSPS st1_cc<2:0> = "001" st2_cc<2:0> = "001"	-	2.1	-	mW
		$F_S=4$ MSPS st1_cc<2:0> = "001" st2_cc<2:0> = "001"	-	2.5	-	mW
DC accuracy						
Resolution	N	-	-	12	-	bit
Digital inputs and outputs						
Input logic coding			Offset binary			code
High level input voltage	V_{IH}	-	$0.7V_{dd25}$	-	-	V
Low level input voltage	V_{IL}	-	-	-	$0.3V_{dd25}$	V
Analog inputs						
Differential full-scale range	$A_{IN\ p-p}$	-	-	2	-	V
Input common-mode voltage	$V_{cm\ in}$	-	-	1.25	-	V
Timing information						
Input clock	F_{clk}	-	1	-	52	MHz
Sampling rate	F_S	-	0.1	-	4	MSPS
Duty cycle	S	-	45	-	55	%

Table “Electrical characteristics” (continue)

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
External reference requirements						
Reference current	I_{ref}	-	9.9	10	10.1	uA
Positive voltage reference	V_{refp}	-	-	1.75	-	V
Common-mode voltage reference	V_{cm}	-	-	1.25	-	V
Negative voltage reference	V_{refn}	-	-	0.75	-	V
Dynamic characteristics at $F_s = 1.5$ MSPS						
Signal-to-noise ratio	SNR	$f_{in} = 1.9$ MHz	-	57.3	-	dB
		$f_{in} = 5$ MHz	-	57.4	-	dB
		$f_{in} = 10.7$ MHz	-	55.4	-	dB
Signal-to-noise and distortion ratio	SINAD	$f_{in} = 1.9$ MHz	-	56.7	-	dB
		$f_{in} = 5$ MHz	-	57.2	-	dB
		$f_{in} = 10.7$ MHz	-	55.3	-	dB
Effective number of bits	ENOB	$f_{in} = 1.9$ MHz	-	9.1	-	bits
		$f_{in} = 5$ MHz	-	9.2	-	bits
		$f_{in} = 10.7$ MHz	-	8.9	-	bits
Spurious-free dynamic range	SFDR	$f_{in} = 1.9$ MHz	-	66.4	-	dB
		$f_{in} = 5$ MHz	-	70.2	-	dB
		$f_{in} = 10.7$ MHz	-	70.9	-	dB
Dynamic characteristics at $F_s = 2.5$ MSPS						
Signal-to-noise ratio	SNR	$f_{in} = 1.9$ MHz	-	55.8	-	dB
		$f_{in} = 5$ MHz	-	56.2	-	dB
		$f_{in} = 10.7$ MHz	-	54.7	-	dB
Signal-to-noise and distortion ratio	SINAD	$f_{in} = 1.9$ MHz	-	55.5	-	dB
		$f_{in} = 5$ MHz	-	56.0	-	dB
		$f_{in} = 10.7$ MHz	-	54.6	-	dB
Effective number of bits	ENOB	$f_{in} = 1.9$ MHz	-	9.0	-	bits
		$f_{in} = 5$ MHz	-	9.1	-	bits
		$f_{in} = 10.7$ MHz	-	8.8	-	bits
Spurious-free dynamic range	SFDR	$f_{in} = 1.9$ MHz	-	65.7	-	dB
		$f_{in} = 5$ MHz	-	69.0	-	dB
		$f_{in} = 10.7$ MHz	-	69.1	-	dB
Dynamic characteristics at $F_s = 4$ MSPS						
Signal-to-noise ratio	SNR	$f_{in} = 5$ MHz	-	52.5	-	dB
		$f_{in} = 10.7$ MHz	-	53.5	-	dB
Signal-to-noise and distortion ratio	SINAD	$f_{in} = 5$ MHz	-	52.4	-	dB
		$f_{in} = 10.7$ MHz	-	53.5	-	dB
Effective number of bits	ENOB	$f_{in} = 5$ MHz	-	8.4	-	bits
		$f_{in} = 10.7$ MHz	-	8.6	-	bits
Spurious-free dynamic range	SFDR	$f_{in} = 5$ MHz	-	69.5	-	dB
		$f_{in} = 10.7$ MHz	-	71.1	-	dB

8 TYPICAL CHARACTERISTICS

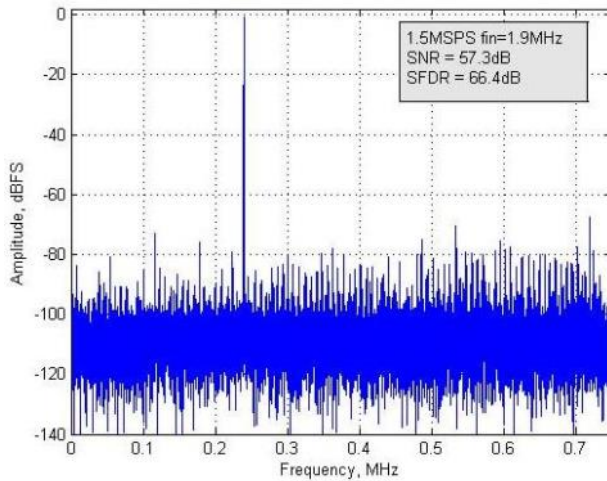


Figure 3: Spectrum with $F_S=1.5$ MSPS and $f_{in}=1.9$ MHz

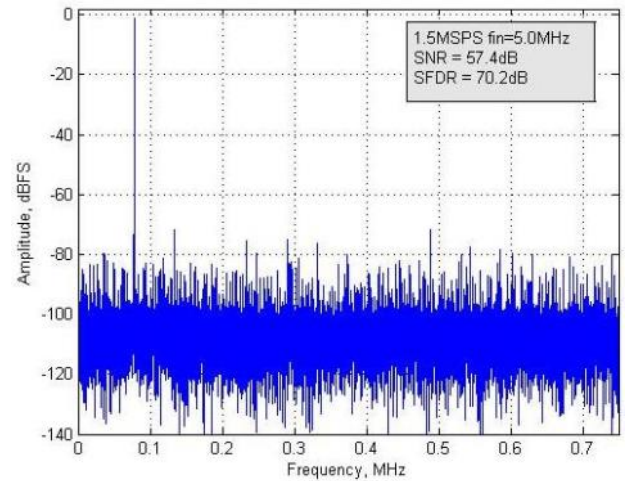


Figure 4: Spectrum with $F_S=1.5$ MSPS and $f_{in}=5$ MHz

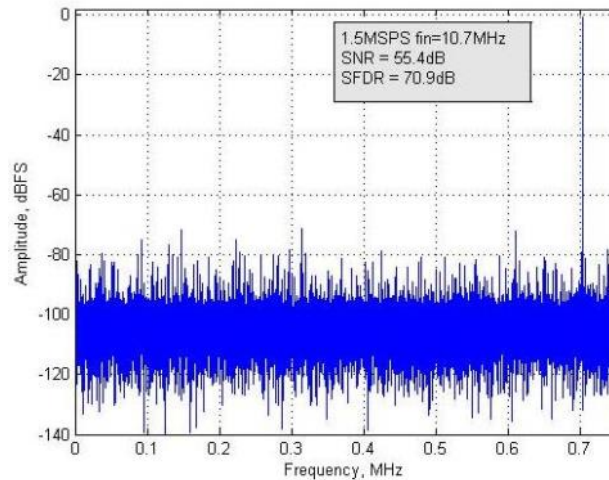


Figure 5: Spectrum with $F_S=1.5$ MSPS and $f_{in}=10.7$ MHz

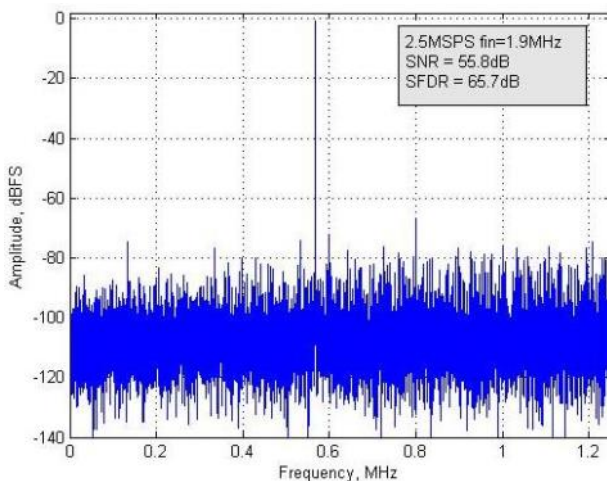


Figure 6: Spectrum with $F_S=2.5$ MSPS and $f_{in}=1.9$ MHz

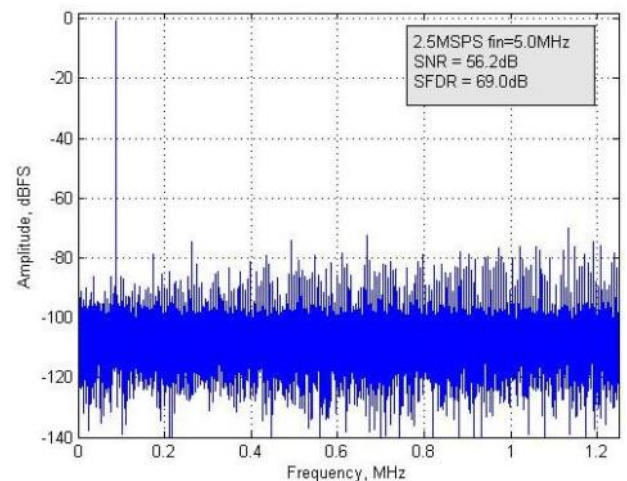


Figure 7: Spectrum with $F_S=2.5$ MSPS and $f_{in}=5$ MHz

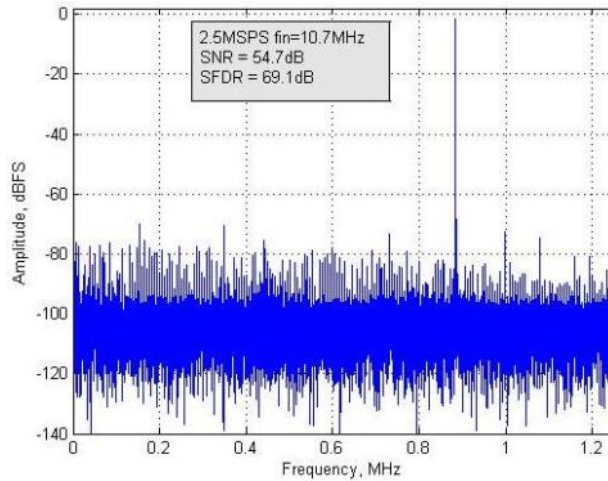


Figure 8: Spectrum with $F_S=2.5$ MSPS and $f_{in}=10.7$ MHz

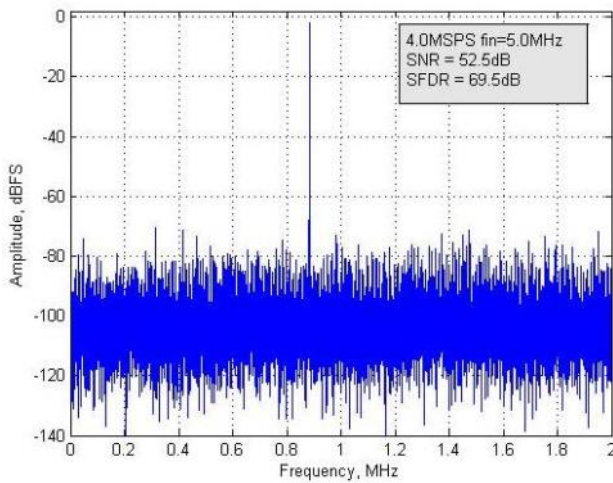


Figure 9: Spectrum with $F_S=4$ MSPS and $f_{in}=5$ MHz

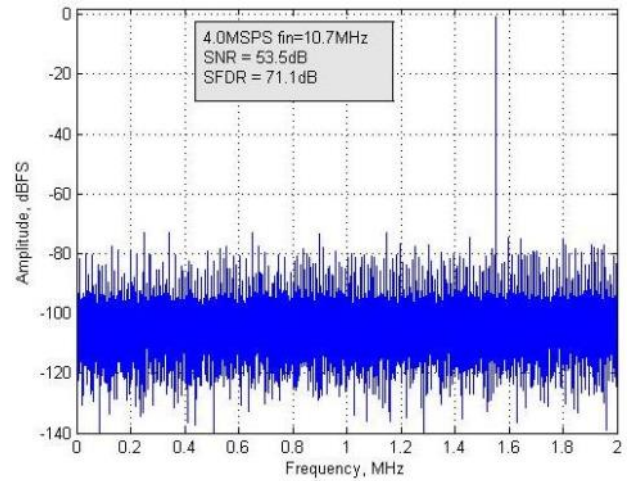


Figure 10: Spectrum with $F_S=4$ MSPS and $f_{in}=10.7$ MHz

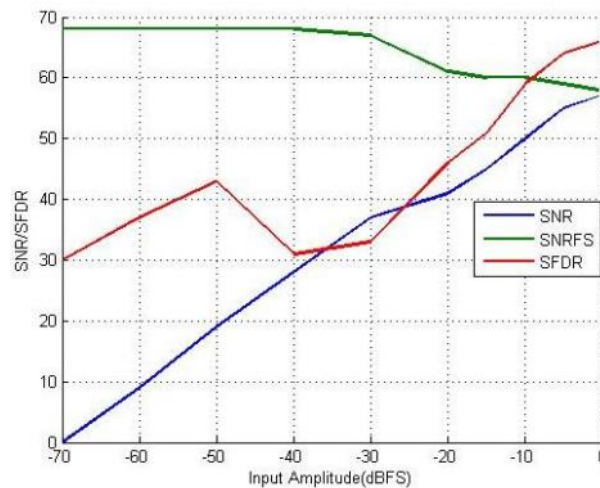


Figure 11: SNR/SFDR vs. input amplitude with $F_S=1.5$ MSPS and $f_{in}=1.9$ MHz

9 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Layout or blackbox
- Verilog, lef and lib files
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

1. From version 1.0:
 - Section 1 was changed (refer to page 1)
 - Section 3 was changed (refer to page 1)
 - Subsection 7.2 was changed (refer to page 5)
2. From version 1.1:
 - Section 6 was changed (refer to page 4)
 - Subection 7.2 was changed