5 MHz 14-bit 2 channel 300 kSPS cascade delta-sigma ADC

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- Cascade (2-2) delta-sigma ADC
- Supply voltage from 1.3 V to 3.0 V
- Input differential signal range – 0.64 V
- LDO embedded
- Internal reference voltage generation (0.6 V ± 0.2 V)
- Supported foundries: TSMC, Global Foundries

2 APPLICATION

- Analog to digital conversion of the signal
- Receivers, transceivers
- Measurement environment
- Medicine environment

3 OVERVIEW

The block is fourth order cascade (2-2) delta-sigma ADC with 5-level quantizers in both stages. The block consists of:

- two delta-sigma modulators second order, coupled in series, in each channel
- clock generator
- bias current source
- voltage reference source
- CLA-, DWA-, BiDWA-correction of capacitors' mismatch
- digital filter

ADC is designed for TSMC CMOS 65 nm technology using 6 levels of metal wiring.

4 STRUCTURE

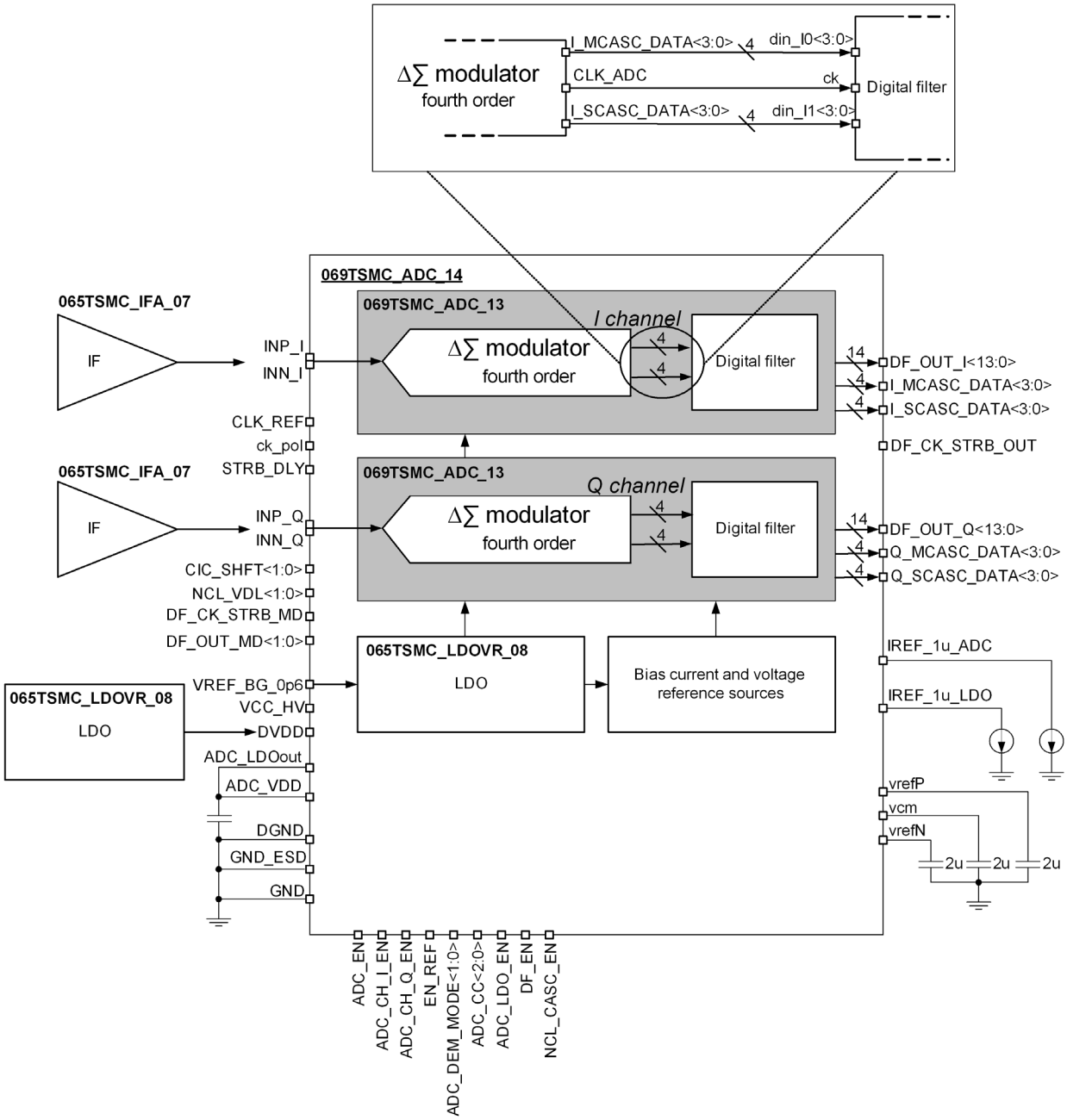

Figure 1: ADC application diagram

5 PIN DESCRIPTION

Name	Direction	Description
Delta-sigma modulator		
IREF_1u_LDO	I	LDO reference current (effluent) 1 uA
IREF_1u_ADC	I	ADC reference current (effluent) 1 uA
VREF_BG_0p6	I	Reference voltage 0.6 V
EN_REF	I	Reference voltage source enable: “0” disable “1” enable (default)
ADC_LDO_EN	I	LDO enable: “0” disable “1” enable (default)
ADC_EN	I	ADC enable: “0” disable “1” enable (default)
ADC_CH_I_EN	I	I channel ADC enable, if ADC_EN = “1”: “0” disable “1” enable (default)
ADC_CH_Q_EN	I	Q channel ADC enable, if ADC_EN = “1”: “0” disable “1” enable (default)
INP_I INN_I	I	I channel input differential signal
INP_Q INN_Q	I	Q channel input differential signal
ADC_CC<2:0>	I	ADC bias current control: “000” 0.5 uA “001” 1.0 uA (default) … with step of 0.5 uA “111” 4.0 uA
CLK_REF	I	Reference clock signal 5 MHz
ADC_DEM_MODE<1:0>	I	Correction of capacitor mismatch mode: “00” without correction “01” CLA “10” DWA “11” BiDWA (default)
CLK_ADC	O	ADC clock output
vrefP vrefN	P	Differential reference voltages
vcm	P	Common mode reference voltage
I_MCASC_DATA<3:0>	O	I channel ADC main cascade (cascade 0) output data
I_SCASC_DATA<3:0>	O	I channel ADC second cascade (cascade 1) output data of
Q_MCASC_DATA<3:0>	O	Q channel ADC main cascade (cascade 0) output data of
Q_SCASC_DATA<3:0>	O	Q channel ADC second cascade (cascade 1) output data of

Table "Pin description" (continue)

Name	Direction	Description
ADC_LDOout	P	LDO output 1.2 V
ADC_VDD	P	Analog blocks supply voltage 1.2 V
VCC_HV	P	External LDO supply voltage 1.3–3.0 V
GND	P	Analog blocks ground
GND_ESD	P	Ground for electrostatic discharge protection
Digital filter		
nrst	I	Digital filter reset: “0” reset “1” active mode (default)
ck_pol	I	Polarity of the digital filter clock signal: “0” direct (default) “1” inverse
ck	I	Digital filter clock input
DF_EN	I	Digital filter enable: “0” disable “1” enable (default)
din_I0<3:0>	I	Digital filter input data from ADC I channel main cascade (cascade 0)
din_I1<3:0>	I	Digital filter input data from ADC I channel second cascade (cascade 1)
din_Q0<3:0>	I	Digital filter input data from ADC Q channel main cascade (cascade 0)
din_Q1 <3:0>	I	Digital filter input data from ADC Q channel second cascade (cascade 1)
NCL_CASC_EN	I	Quantization noise compensation enable: “0” disable “1” enable (default)
DF_OUT_MD<1:0>	I	Output signal mode: “00” noise cancellation circuit output
		“01” first cascade of digital filter output data, decimation coefficient is 4
		“10” second cascade of digital filter output data, decimation coefficient is 8
		“11” third cascade of digital filter output data (main output), decimation coefficient is 16 (default)
DF_CK_STRB_MD	I	Output data synchronization mode: “0” synchronization by rising edge of DF_CK_STRB_OUT (default) “1” synchronization by rising edge of CLK_ADC
CIC_SHFT<1:0>	I	CIC filter gain: “00” ×1 “01” ×2 “10” ×4 “11” ×8 (default)

Table "Pin description" (continue)

Name	Direction	Description
NCL_VDL<1:0>	I	The clock delay value of main stage with respect to the second stage in noise cancellation circuit: “00” 0 “01” 1 “10” 2 (default) “11” 3
STRB_DLY	I	Synchronization correction register in digital filtering block
DF_CK_STRB_OUT	I	Synchronization signal of output data
DF_OUT_I<13:0>	O	I channel digital filter output
DF_OUT_Q<13:0>	O	Q channel digital filter output
DVDD	P	Digital filter supply voltage 1.2V
DGND	P	Digital filter ground

6 FUNCTIONAL DESCRIPTION

ADC can operate in two modes: standby mode and active mode, which could be selected by logic levels at ADC_EN and DF_EN inputs:

- ADC_EN = “0”, DF_EN = “0”: Standby mode. Analog blocks and digital filter are disabled; LDO and voltage reference source are enabled. Low power consumption
- ADC_EN = “1”, DF_EN = “1”: Active mode. Analog blocks end filter are enabled; High power consumption

After power on supply, ADC_EN, DF_EN, EN_IF, ADC_LDO_EN, ADC_CH_I_EN, ADC_CH_Q_EN inputs should be enabled by high level voltage (logic “1”) and at least 6 ms should pass for voltage reference stabilization.

After disable of standby mode, at least 50 us should pass to stabilize signal at the output of ADC.

Delta-sigma modulator includes capacitor mismatch correction circuit. This block implements CLA (Clocked Averaging), DWA (Data Weighted Averaging), BiDWA (Bi-directional Data Weighted Averaging) algorithms. ADC operation without using correction algorithm is also possible.

Due to process variations, synchronization errors of the internal system clock of the digital filter could appear. To overcome this it is recommended to add an additional time shift in the internal clock by high voltage level (logic “1”) at input STRB_DLY. Timing diagram of ADC module is shown in Figure 2.

The digital filter is clocked by delta-sigma modulator (CLK_ADC output). Synchronization of output data could be carried out in two ways, depending on the logic level in DF_CK_STRB_MD input:

- DF_CK_STRB_MD = “0”: synchronization by rising edge of DF_CK_STRB_OUT
- DF_CK_STRB_MD = “1”: synchronization by rising edge of CLK_ADC

Output signal is presented in 14-bit binary code at output of the digital filter. The direct data of delta-sigma modulator is also available in 8 bit (4 bit per cascade) thermometer code.

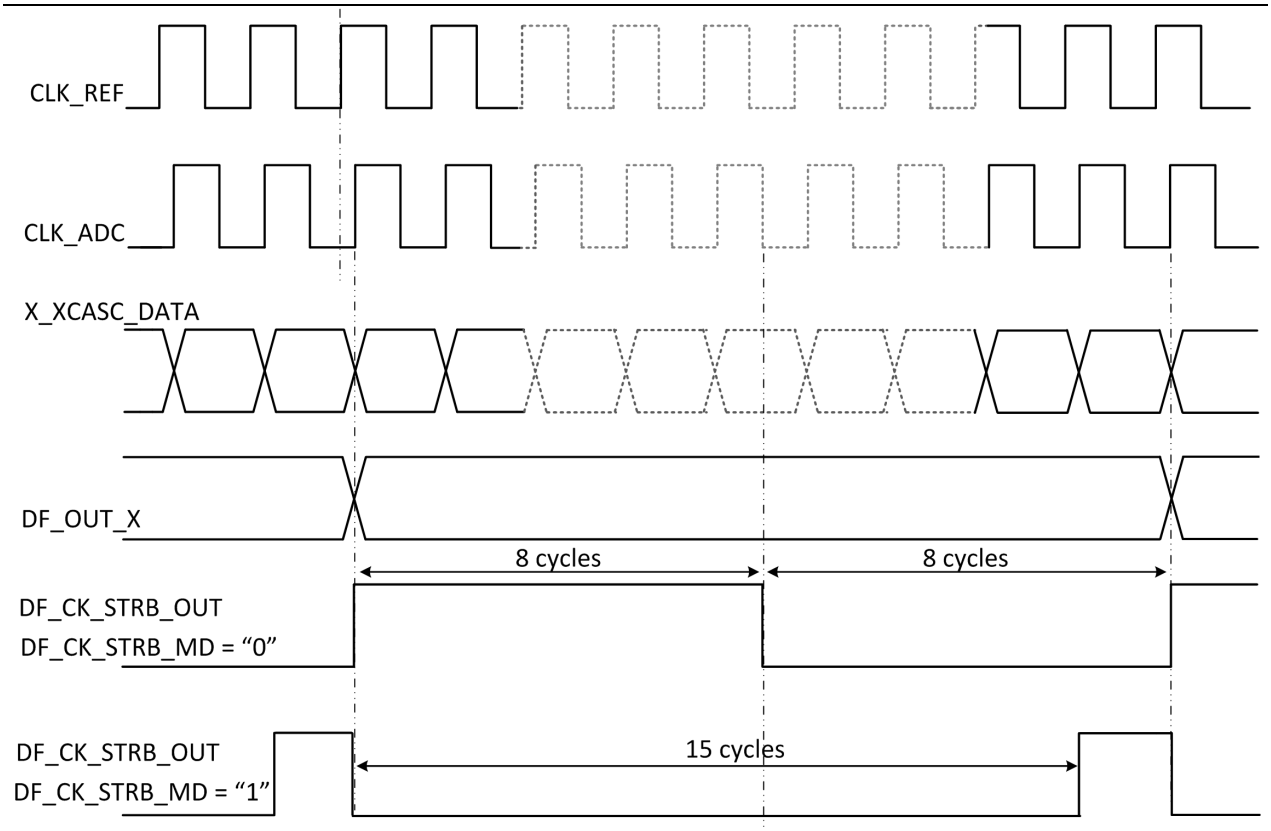

Figure 2: Timing diagram

7 LAYOUT DESCRIPTION

Table 1: Delta-sigma modulator dimensions

Dimension	Value	Unit
Height	730	um
Width	870	um

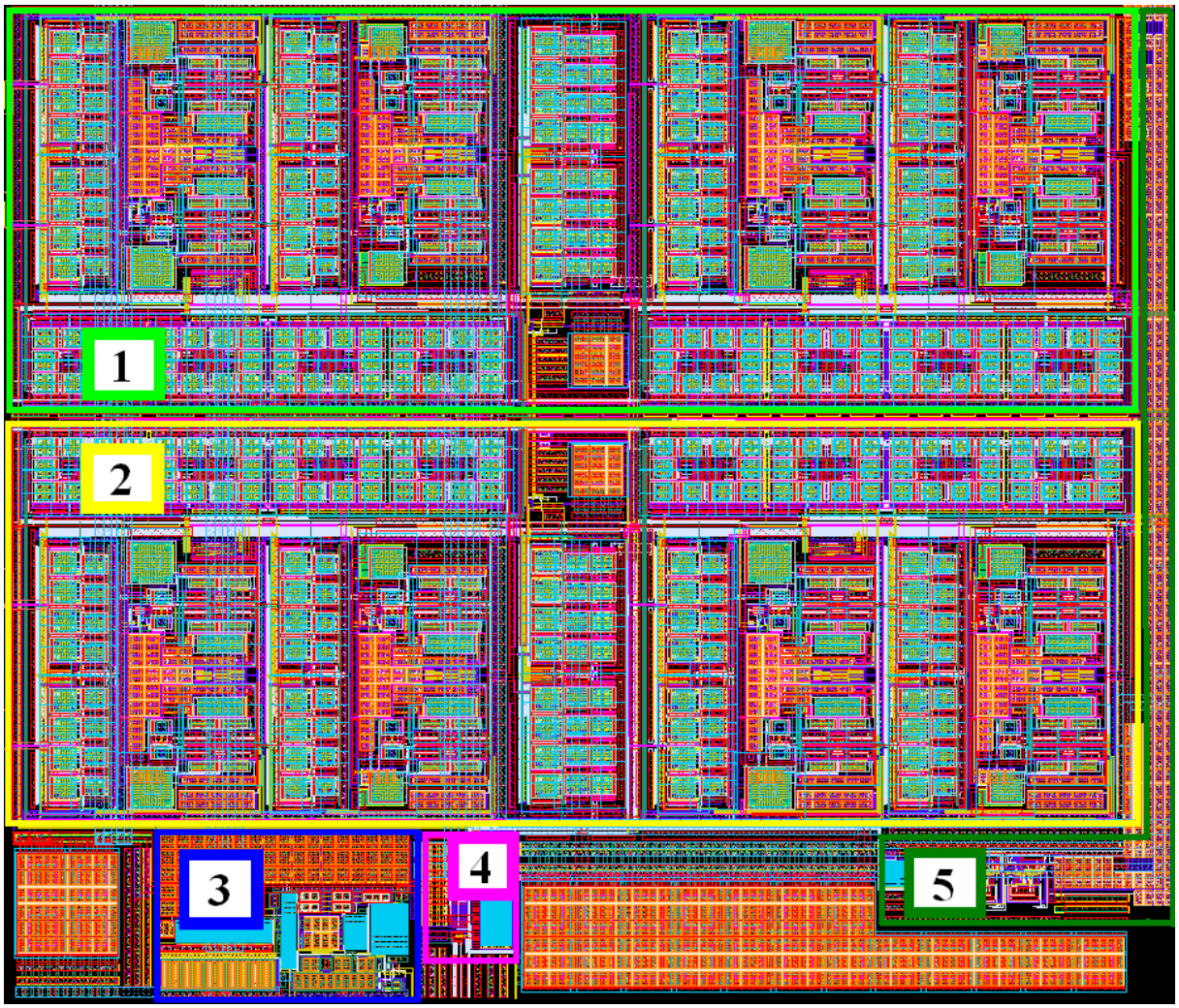

Figure 3: Delta-sigma modulator layout

1. I channel delta-sigma modulator
2. Q channel delta-sigma modulator
3. Low drop out voltage regulator (LDO)
4. Bias current source
5. Voltage reference source
6. Capacitors

8 INTEGRATION GUIDELINES

Input differential signal connects to INP_I and INN_I inputs for I channel (INP_Q and INN_Q for Q channel). Signal sources should be located as close as possible to ADC inputs to minimize parasitic influence of neighbor blocks and wiring.
vrefP, vrefN, vcm inputs should be connecting with external capacitors of nominal value of 2 uF for stabilizing voltage reference.
Clock signal should be connected to input CLK_REF. It must have rising/falling edge no more than 1ns. Transitions are measured at levels 0.1*VDD and 0.9*VDD.
Control inputs (EN_IF, ADC_LDO_EN, ADC_EN, ADC_CH_I_EN, ADC_CH_Q_EN, ADC_DEM_MODE<1:0>, ADC_CC_<2:0>) should have rising/falling edge no more than 5 ns. They are used to select operating mode and are the same when ADC is used.

8.1 PLACEMENT AND ROUTING

The following requirements of placement and routing must be satisfied during integration:

- No routing and placement of any topological elements are allowed over the block
- Power supplies (pin ADC_VDD, VCC_HV, ADC_LDOout) and ground (pin GND) wires for analog blocks must allow flowing of 2 mA current (6mA peak current) and should have total resistance of less than 2 Ohm each
- Power supply (pin DVDD) and ground (pin DGND) wires for digital blocks must allow flowing of 0.8 mA current (3 mA peak current) and should have total resistance of less than 5 Ohm each
- The minimum distance between analog part of ADC (delta-sigma modulator), and neighboring blocks must be 10-15 um. It is recommended to fill the space between GND and ADC_VDD by the filter capacitors
- Do not place high-frequency and noisy circuits close to analog part of ADC
- It is recommended to surround the block of delta-sigma modulator by deep n-well guard ring
- It is recommended to surround the digital block by deep n-well guard ring
- The length of output wires of delta-sigma modulator (I_MCASC_DATA<3:0>, I_SCASC_DATA<3:0>, Q_MCASC_DATA<3:0>, Q_SCASC_DATA<3:0>) must be of less than 250 um. Their resistance should be of less than 100 Ohms for each and total capacity (including parasitic) should be of less than 1.5 pF each

9 OPERATING CHARACTERISTICS

9.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 65 nm
Status silicon proven
Area of delta-sigma modulator 0.64 mm^2
Area of the digital filter 0.083 mm^2
Total area 0.723 mm^2

9.2 ELECTRICAL CHARACTERISTICS

The values of electrical parameters are given for V_{HV} = 1.3 ÷ 3.0 V, DVDD = 1.08 ÷ 1.32 V and Tj = -40 ÷ +85°C; typical values are at V_{HV} = 2.5 V, DVDD = 1.2 V and Tj = 27° C, unless otherwise specified

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Operating temperature	Tj	-	-40	27	+85	°C
External high supply voltage (VCC_HV)	V_{HV}	-	1.3	2.5	3.0	V
Digital filter supply voltage	DVDD	-	1.08	1.2	1.32	V
Delta-sigma modulator output voltage (ADC_VDD)	V_{DSM}	-	1.14	1.2	1.26	V
Delta-sigma modulator current consumption	I_{DSM}	One channel	0.21	0.23	0.36	mA
		Two channels	0.37	0.41	0.64	
Reference source current consumption	I_{VREF}	-	67	75	220	uA
Digital filter current consumption	I_{DVDD}	-	150	200	250	uA
Clock frequency	F_{clk}	-	-	5	-	MHz
Oversampling ratio	OSR	-	-	16	-	-
Bandwidth	BW	-	-	150	-	kHz
Signal to noise ratio	SNR	BW = 150 kHz	60	67	72	dB
Spurious free dynamic range	SFDR	-	-	78	-	dB
Clock input duty cycle	S	-	45	50	55	%
Clock signal period jitter	T_{JIT}	-	-	50	-	ps
Input differential signal range	$V_{dif\ p\text{-}p}$	-	-	0.64	-	V
Common mode voltage	vcm	-	-	0.6	-	V
Differential reference voltage	vrefP	-	-	0.8	-	V
	vrefN	-	-	0.4	-	
Input logic high level	V_{IH}	For digital inputs	$0.8V_{HV}$	-	V_{HV} +0.1	V
Input logic low level	V_{IL}		-0.1	-	$0.2V_{HV}$	V
Output logic high level	V_{OH}	-	-	DVDD	-	V
Output logic low level	V_{OL}	-	-	0	-	V

9.3 DYNAMICAL CHARACTERISTICS

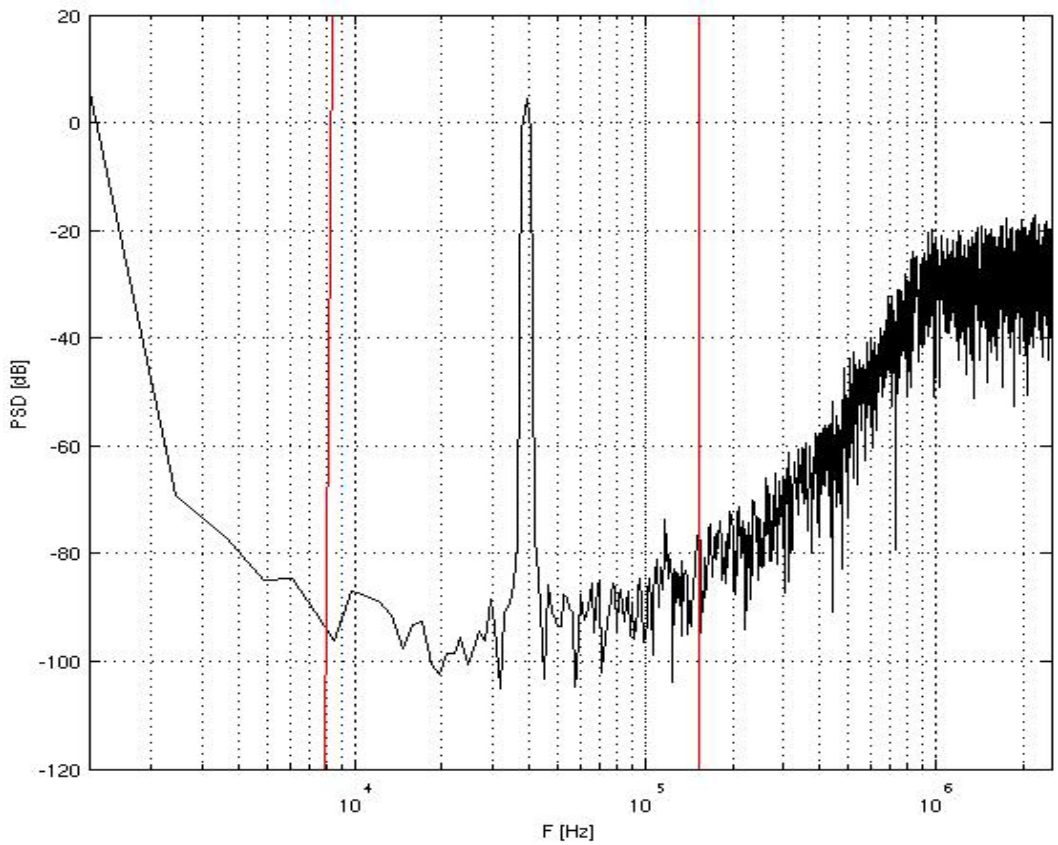

Figure 4: Delta-sigma modulator output signal spectrum

10 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

11 REVISION HISTORY

From version 1.0:

- Subsection 9.1 updated:
  - Digital filter area value was changed from 0.76 to 0.083 mm^2
- Subsection 9.2 updated:
  - Digital filter current consumption value was changed