14-bit 1-channel 50 MSPS pipeline ADC

SPECIFICATION

1 FEATURES

- TSMC CMOS 90nm
- Resolution 14 bit
- Sampling rate up to 50 MSPS
- Using different power supply 1 V for digital and 1.8 V for analog parts of ADC circuitry
- Standby mode (current consumption 5 uA)
- Power dissipation from 62 mW to 314.2 mW
- Spurious-free dynamic range 62 dB
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Optical networking
- Test equipment
- Portable ultrasound and digital beam-forming systems
- Telecommunication systems
- Higher quality imaging in video systems

3 OVERVIEW

This ADC has architecture of pipelined ADC, pipeline ADC consists of a cascade of stages, each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (multiplying digital-to-analog converter, MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. This ADC consist of: bias, lvds clock receiver, ADC core, output logic correction block. The ADC requires 1.6 ÷ 2 V analog supply and 0.9 ÷ 1.1 V digital supply, there are standby mode which allow to optimize power consumption for system need. Also exist tuning of ADC operating mode by digital correction registers: register ref<3:0> specify differential reference range (refp and refn), register iadc<2:0> specify tuning of ADC currents, register ish<2:0> specify tuning of sample-and-hold currents, exist possibility to use external voltage source for differential reference refp and refn.
The device is implemented on TSMC CMOS 90nm technology.

4 STRUCTURE

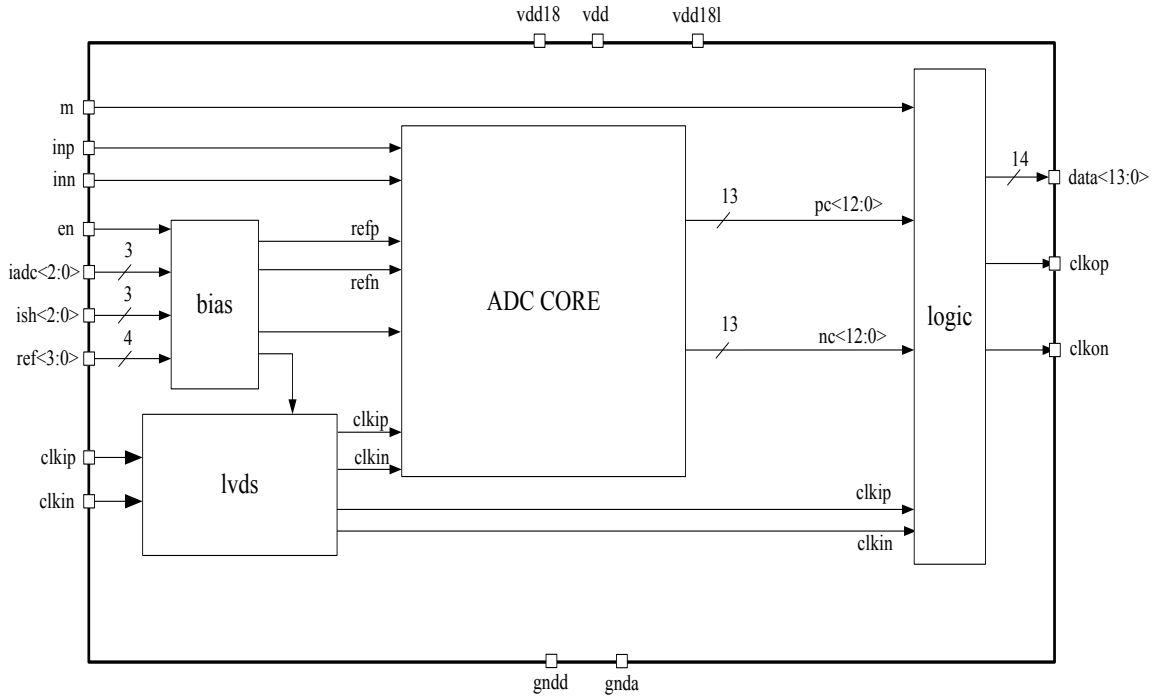

Figure 1: 14-bit 1-channel 50 MSPS pipeline ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
en	I	Enable
inp	I	Differential analog input
inn		
clkp	I	Differential input clock
clkn		
ref<3:0>	I	Tuning register of differential reference
iadc<2:0>	I	Tuning current register of ADC
ish<2:0>	I	Tuning current register of sample-and-hold circuit
m	I	Selection register of type output code
data<13:0>	O	Output data line
clkop	O	Differential output clock
clkon		
refp	I/O	Differential reference
refn		
vdd18	I/O	Analog blocks supply voltage 1.8 V
vdd18l	I/O	Analog blocks supply voltage 1.8 V
vdd	I/O	Digital blocks supply voltage 1 V
gnda	I/O	Analog blocks ground
gndd	I/O	Digital blocks ground

6 LAYOUT DESCRIPTION

Analog-to-digital converter layout dimensions are given in the table 1.

Table 1: Block dimensions of the 14-bit ADC.

Dimension	Value	Unit
Height	1807	um
Width	465	um

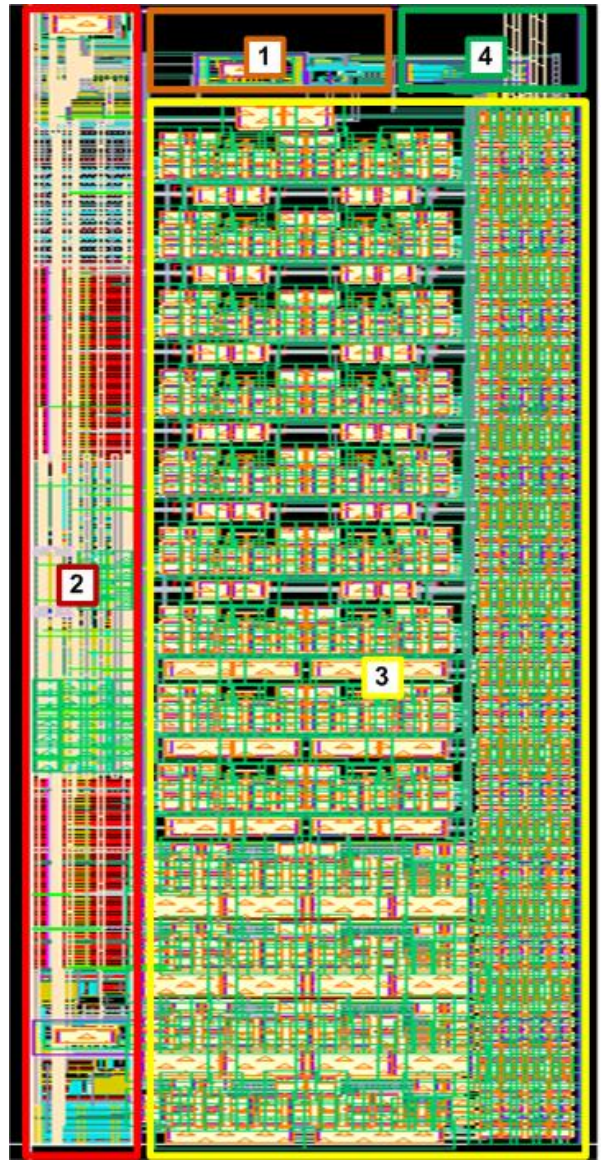

Figure 2: 14-bit ADC layout view

1. LVDS clock receiver
2. Bias
3. ADC core
4. Output logic

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 90nm
Status silicon proven
Area 0.84 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd18} = 1.6 ÷ 1.8 V, V_{dd}=0.9 ÷ 1.1 V, T = -60 ÷ +125°C. Typical values are at V_{dd18} = 1.8 V, V_{dd} = 1.0 V, T = +27°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Operating temperature range	T	-	-60	27	125	°C
Analog blocks supply voltage	V_{dd18},V_{dd18l}	-	1.6	1.8	2	V
Digital blocks supply voltage	V_{dd}	-	0.9	1.0	1.1	V
Resolution	N	-	-	14	-	bit
Sampling rate	F_s	-	-	50	-	MSPS
Bandwidth	F_b	-	-	25	-	MHz
Stand-by current	I_{st}	-	-	5	-	uA
Current consumption	I_{cn}	-	-	176.8	-	mA
Maximum amplitude of input signal	A_{IN}	-	1.02	1.024	1.03	V
Reference voltages for the input signal	V_{REF+}	-	1.31	1.43	1.51	V
	V_{REF-}		0.37	0.41	0.44	V
Analog input voltage range	$A_{IN\ p-p}$	-	-	2	-	V
Input common mode voltage range	U	-	$0.5V_{dd18}$ - 100mV	$0.5V_{dd18}$	$0.5V_{dd18}$ +100mV	V
Total harmonic distortion	THD	Input amplitude of 0.9 from full scale (A_{IN}), input frequency 1.56 MHz, F_{clk} = 50 MHz	-	-60.5	-	dB
Signal-to-noise ratio	SNR		-	58	-	dB
Spurious-free dynamic range	SFDR		60	62	64	dB
Input logic-level high	V_{IH}	For digital inputs	0.7	-	-	V
Input logic-level low	V_{IL}		-	-	0.3	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation