10-bit 1-channel 1 MSPS SAR ADC

SPECIFICATION

1 FEATURES

- TSMC CMOS 90 nm
- Resolution 10 bit
- Using different power supply 1 V for digital and 3.3 V for analog parts of ADC circuitry
- Standby mode (current consumption 230 nA)
- Power dissipation from 0.69 mW to 3.08 mW
- Spurious-free dynamic range 65 dB
- Supported foundries: UMC, Global Foundries, SMIC, iHP, Vanguard, SilTerra

2 APPLICATION

- Digital cellular phones
- Portable recording devices
- Digital audio workstations
- Remote sensors
- Data logging devices

3 OVERVIEW

The 10-bit ADC has an architecture of successive approximation analog to digital converter circuit. Successive approximation analog to digital converter consists of four main subcircuits: sample and hold circuit to acquire the input voltage (V_{in}), analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation logic. A successive approximation logic subcircuit designed to supply an approximate digital code of V_{in} to the internal DAC. An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the successive approximation logic for comparison with V_{in}. The successive approximation logic is initialized so that the most significant bit is equal to a digital “1”. This code is fed into the DAC, which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage. If this analog voltage exceeds V_{in} the comparator causes the successive approximation logic to reset this bit; otherwise, the bit is left a “1”. Then the next bit is set to “1” and the same test is done, continuing this binary search until every bit in the successive approximation logic has been tested. The resulting code is the digital approximation of the sampled input voltage and is finally output by the DAC at the end of the conversion. This ADC consist of: input multiplexer block, ADC core, output logic block, clock generator. The ADC core consist of internal DAC, bias, sample and hold circuit, analog voltage comparator. The ADC requires 3.0...3.6 V analog supply and 0.9...1.1 V digital supply voltage, there are standby mode which allow to optimize power consumption for system need.
The device is implemented on TSMCCMOS 90nm technology.

4 STRUCTURE

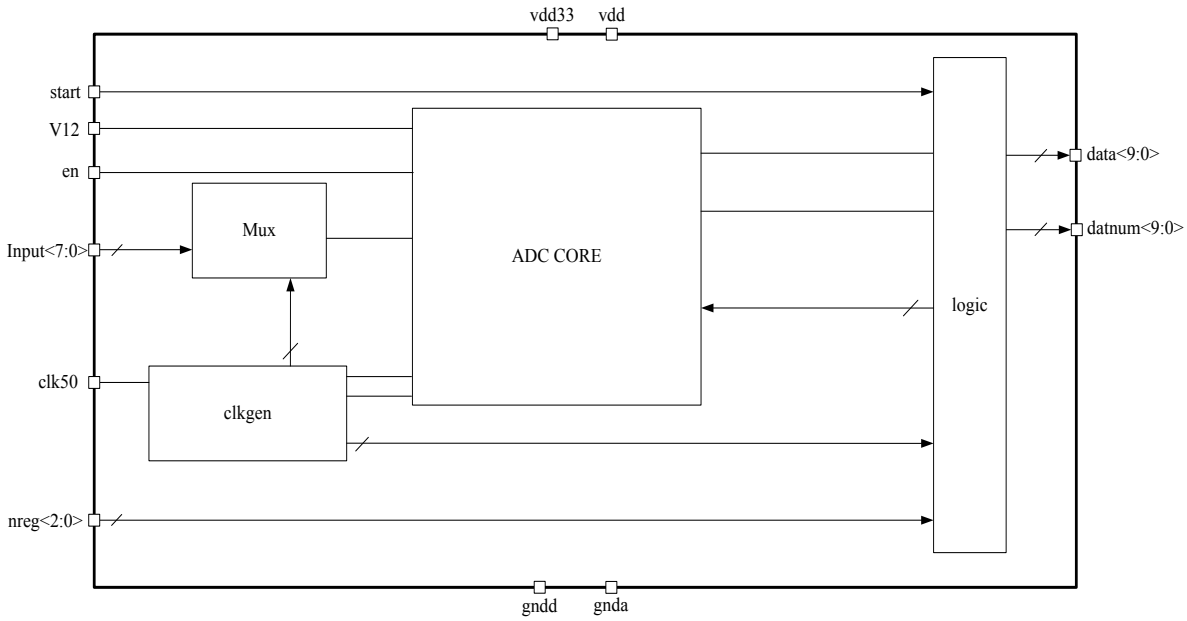

Figure 1: 10-bit 1-channel 1 MSPS SAR ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
en	I	Enable
input<7:0>	I	Input data bus
V12	I	Reference voltage 1.2 V
clk_50	I	Sampling frequency 50 MHz
nreg<2:0>	I	Selection register of conversion channel
start	I	Start conversion
data<9:0>	O	Output data bus
datnum<9:0>	O	Output engineering bus
vdd33	I/O	Analog blocks supply voltage 3.3 V
vdd	I/O	Digital blocks supply voltage 1 V
gnda	I/O	Analog blocks ground
gndd	I/O	Digital blocks ground

6 LAYOUT DESCRIPTION

Analog-to-digital converter layout dimensions are given in the table 1.

Table 1: Block dimensions of the 10-bit ADC.

Dimension	Value	Unit
Height	145	um
Width	308	um

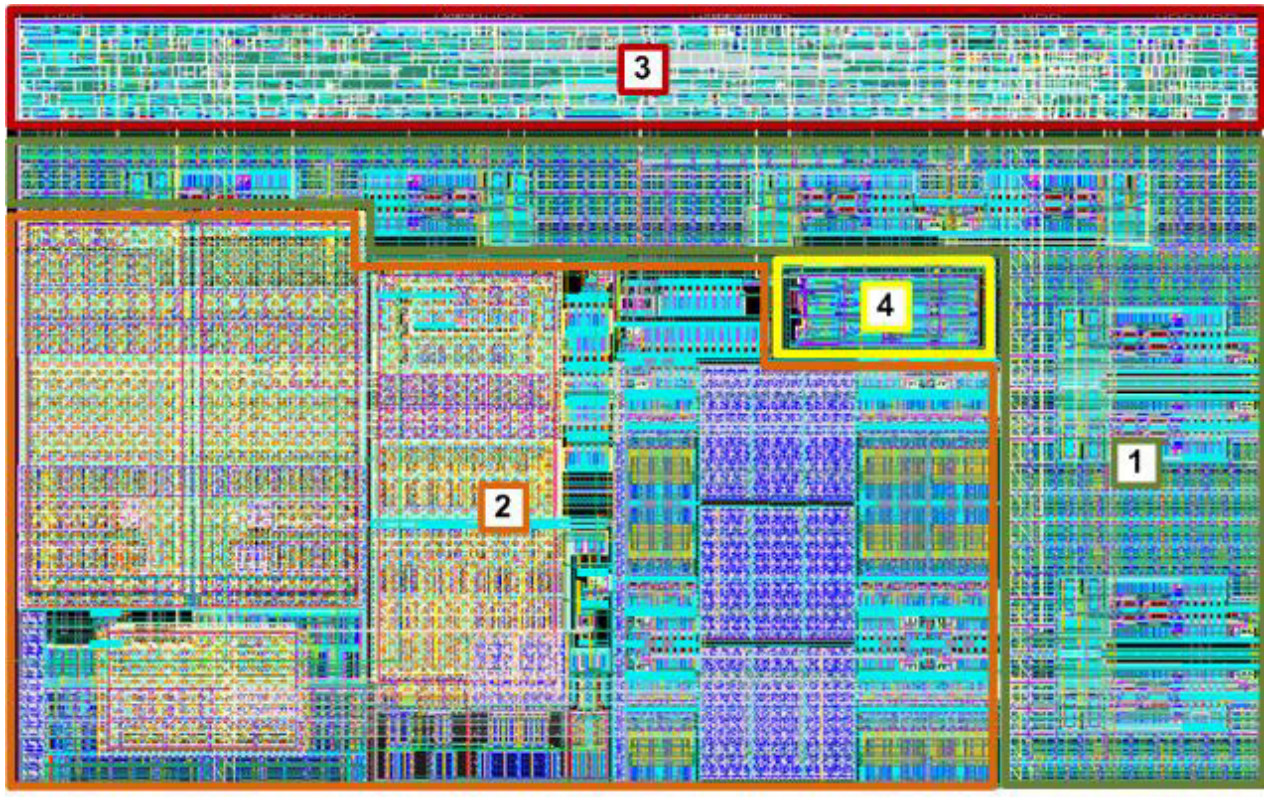

Figure 2: 10-bit ADC layout view

1. Multiplexer
2. ADC core
3. Output logic
4. Clock generator

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 90nm
Status silicon proven
Area 0.045 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd33}= 3.0÷3.6 V, T = -60÷+125°C, V_{dd}=+0.9÷+1.1 V. Typical values are V_{dd33} = +3.3 V, V_{dd}=+1V, T =+27°C and registers meaning, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Operating temperature range	T	-	-60	27	125	°C
Analog blocks supply voltage	V_{dd33}	-	3.0	3.3	3.6	V
Digital blocks supply voltage	V_{dd}	-	0.9	1	1.1	V
Resolution	N	-	-	10	-	bit
Clock frequency	F_{clk}	-	-	50	-	MHz
Sampling rate	F_s	-	-	1	-	MSPS
Bandwidth	F_b	-	-	0.5		MHz
Current consumption in standby mode	I_{st}	-	-	230	-	nA
Power consumption	P_{cn}	-	0.69	1.32	3.08	mW
Spurious-free dynamic range	SFDR	F_{clk} = 50 MHz	65	67	68	dB
High Level Input Voltage	V_{IH}	For digital inputs	0.7	-	-	V
Low Level Input Voltage	V_{IL}		-	-	0.3	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation