

## 14-bit 1-channel 100/125 MSPS ADC

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### SPECIFICATION

#### 1. FEATURES

- TSMC MS CMOS 90 nm
- Resolution 14-bit pipelined ADC
- Sampling rate 100/125 MSPS
- Different power supplies for digital (1 V and 1.8 V) and analog (1.8V) parts
- Low standby current <math><10\mu\text{A}</math>
- Low power dissipation 506 mW
- Spurious-free dynamic range 73dB
- Portable to other technologies (upon request)

#### 2. APPLICATION

- Optical networking
- Test equipment
- Portable ultrasound and digital beam-forming systems
- Telecommunication systems
- High quality imaging video systems

#### 3. OVERVIEW

The high-speed 14-bit ADC employs a high-performance differential pipeline architecture. The ADC consists of a core ADC, LVDS clock receiver, reference voltages and currents circuit. The ADC requires 1.62 ÷ 1.98V analog supply and 0.9 ÷ 1.1V, 1.62 ÷ 1.98V digital supply voltages.

This ADC supports standby mode which allows state with minimum power consumption. There is also the ability to configure the operating modes of the ADC with digital registers: register `ref<3:0>` controls the differential reference voltages, register `ish<3:0>` adjusts current of the sample and hold, register `iadc<3:0>` adjusts current of the core ADC.

The device is manufactured on TSMC MS CMOS 90nm technology.

## 4. STRUCTURE

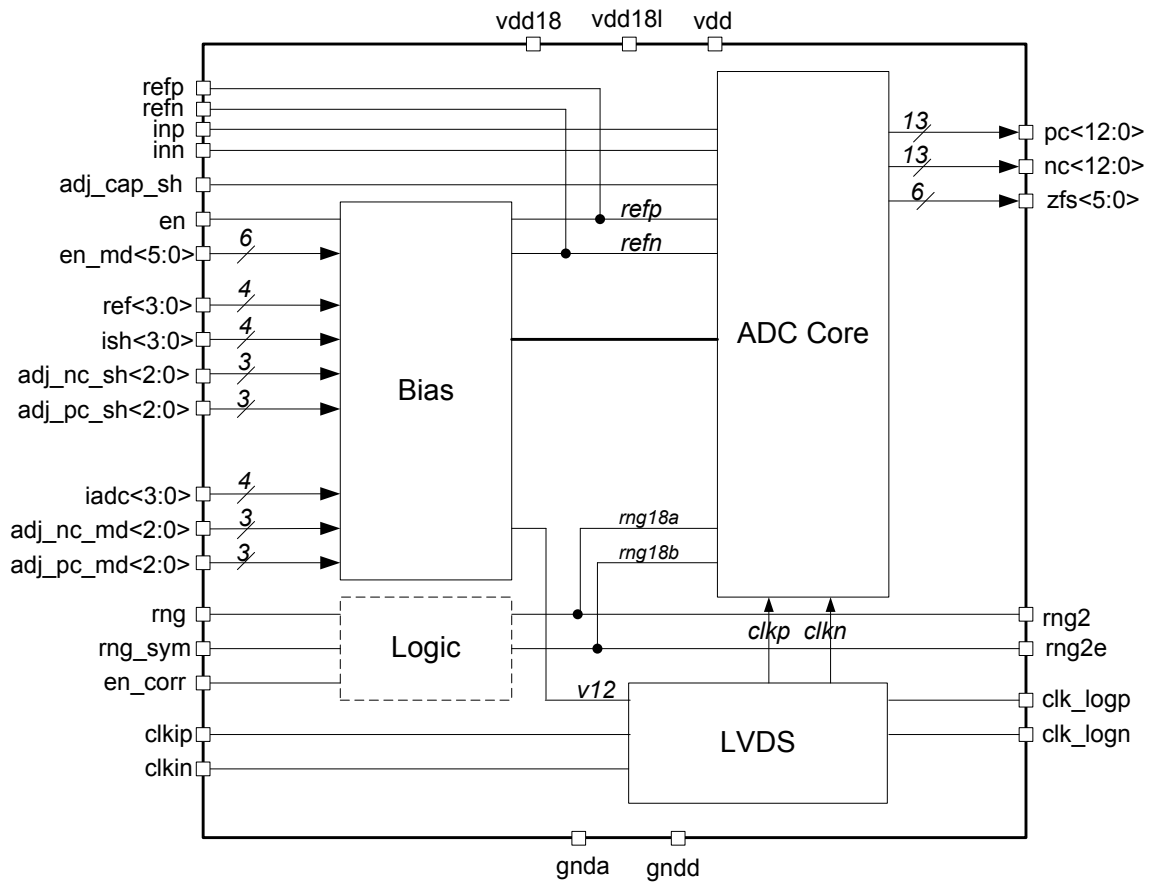


Figure 1: 14-bit 1-channel 100/125 MSPS ADC structure

## 5. PIN DESCRIPTION

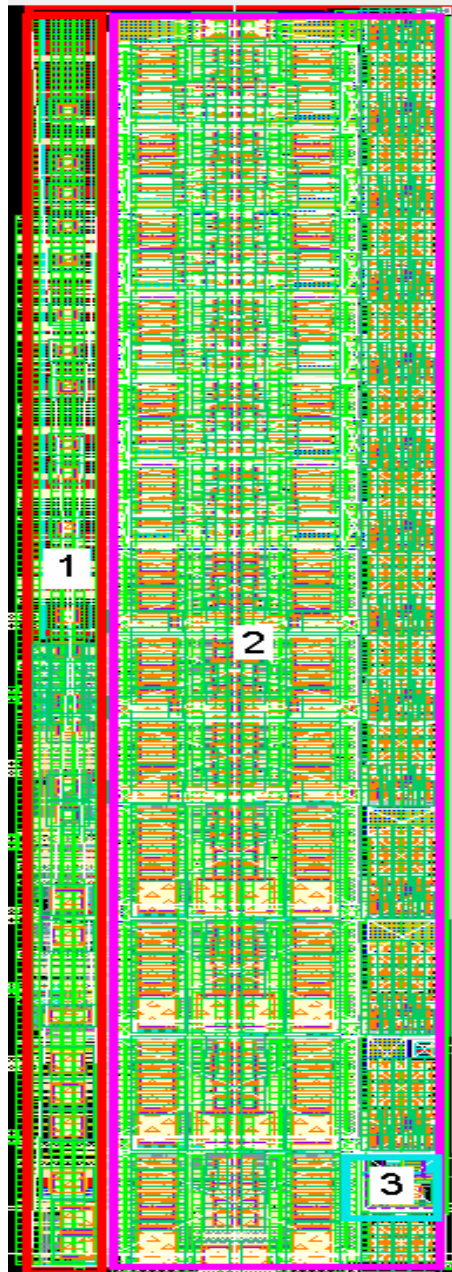
Name	Direction	Description
en	I	Enable/disable ADC
en_corr	I	Enable/disable digital correction
en_md<5:0>	I	Test input
ref<3:0>	I	Differential reference voltage control
ish<3:0>	I	Sample-and-hold circuit Bias control
iadc<3:0>	I	ADC bias control
rng	I	Pseudo-random Input signal
rng_sym	I	Test input
adj_nc_sh<2:0>	I	Test inputs
adj_pc_sh<2:0>	I	
adj_cap_sh	I	
adj_nc_md<2:0>	I	
adj_pc_md<2:0>	I	
clkip	I	Differential clock input
clkin	I	
inp	I	Differential analog input
inn	I	
refp	I/O	Differential reference voltages
refn	I/O	
pc<12:0>	O	Differential output data
nc<12:0>	O	
clk_logp	O	Differential clock output
clk_logn	O	
rng2	O	Pseudo-random output signals for digital correction
rng2e	O	
zfs<5:0>	O	Output data for digital correction
vdd18	I/O	Analog blocks supply voltage 1.8V
vdd18l	I/O	Digital blocks supply voltage 1.8V
vdd	I/O	Digital blocks supply voltage 1V
gnda	I/O	Analog blocks ground
gndd	I/O	Digital blocks ground

## 6. LAYOUT DESCRIPTION

Analog-to-digital converter layout dimensions are given in the table 1.

**Table 1:** Block dimensions of the 14-bit ADC

Dimension	Value	Unit
Height	2340	$\mu\text{m}$
Width	530	$\mu\text{m}$



**Figure 2:** 14-bit ADC layout view

1. Currents and voltages reference
2. ADC core
3. LVDS clock receiver

## 7. OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ TSMC MS CMOS90nm  
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_ 1.24mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{dd18} = 1.62 \div 1.98$  V,  $V_{dd} = 0.9 \div 1.1$  V,  $T = -40 \div +125$ °C. Typical values are at  $V_{dd18} = 1.8$  V,  $V_{dd} = 1.0$  V,  $T = +27$ °C, unless otherwise noted.

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
Analog blocks supply voltage	$V_{dd18}$	-	1.62	1.8	1.98	V
Analog blocks supply voltage	$V_{dd18l}$	-	1.62	1.8	1.98	V
Digital blocks supply voltage	$V_{dd}$	-	0.9	1	1.1	V
Current consumption	$I_{cnVdd18}$	$V_{dd18}$	-	263	-	mA
	$I_{cnVdd18l}$	$V_{dd18l}$	-	17.7	-	mA
	$I_{cnVdd}$	$V_{dd}$	-	25	-	μA
Standby current	$I_{st}$	-	-	10	-	μA
Resolution	N	-	-	14	-	bit
Sample rate	$F_S$	-	-	100/125	-	MSPS
Bandwidth	B	-	-	355	-	MHz
Operating temperature range	T	-	-40	27	125	°C
Reference voltages for the input signal	$V_{REF+}$	-	1.31	1.42	1.51	V
	$V_{REF-}$	-	0.31	0.4	0.47	
Differential peak-to-peak input voltage range	$A_{IN\ d\ p-p}$	-	-	2	-	V
Input common mode voltage	U	-	$0.5V_{dd18} - 100mV$	$0.5V_{dd18}$	$0.5V_{dd18} + 100mV$	V
High level input voltage	$V_{IH}$	Digital inputs	0.7	-	-	V
Low level input voltage	$V_{IL}$		-	-	0.3	V

### 7.3 DYNAMIC CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
$F_S = 100\text{MSPS}$						
Total Harmonic Distortion	THD	$F_{IN} = 1.5625\text{MHz}$ $F_{IN} = 2.3437\text{MHz}$ $F_{IN} = 51.5625\text{MHz}$	–	-71 -58.5 -61	-73	dB
Signal-to-Noise Ratio	SNR	$F_{IN} = 1.5625\text{MHz}$ $F_{IN} = 2.3437\text{MHz}$ $F_{IN} = 51.5625\text{MHz}$	–	62 60.5 58.1	64	dB
Spurious Free Dynamic Range	SFDR	$F_{IN} = 1.5625\text{MHz}$ $F_{IN} = 2.34375\text{MHz}$ $F_{IN} = 51.5625\text{MHz}$	–	73.3 58.9 62.8	76	dB
Signal-to-Noise And Distortion Ratio	SINAD	$F_{IN} = 1.5625\text{MHz}$ $F_{IN} = 2.34375\text{MHz}$ $F_{IN} = 51.5625\text{MHz}$	–	61.5 56.3 56.3	63	dB
$F_S = 125\text{MSPS}$						
Total Harmonic Distortion	THD	$F_{IN} = 1.5625\text{MHz}$ $F_{IN} = 2.34375\text{MHz}$ $F_{IN} = 51.5625\text{MHz}$	–	-65.2 -59.7 -51.8	-70	dB
Signal-to-Noise Ratio	SNR	$F_{IN} = 1.5625\text{MHz}$ $F_{IN} = 2.34375\text{MHz}$ $F_{IN} = 51.5625\text{MHz}$	–	59.2 56.1 54.8	63	dB
Spurious Free Dynamic Range	SFDR	$F_{IN} = 1.5625\text{MHz}$ $F_{IN} = 2.34375\text{MHz}$ $F_{IN} = 51.5625\text{MHz}$	–	66.3 60.3 55.3	71	dB
Signal-to-Noise And Distortion Ratio	SINAD	$F_{IN} = 1.5625\text{MHz}$ $F_{IN} = 2.34375\text{MHz}$ $F_{IN} = 51.5625\text{MHz}$	–	58.3 54.5 50	61	dB

## 8. TYPICAL PERFORMANCE CHARACTERISTICS

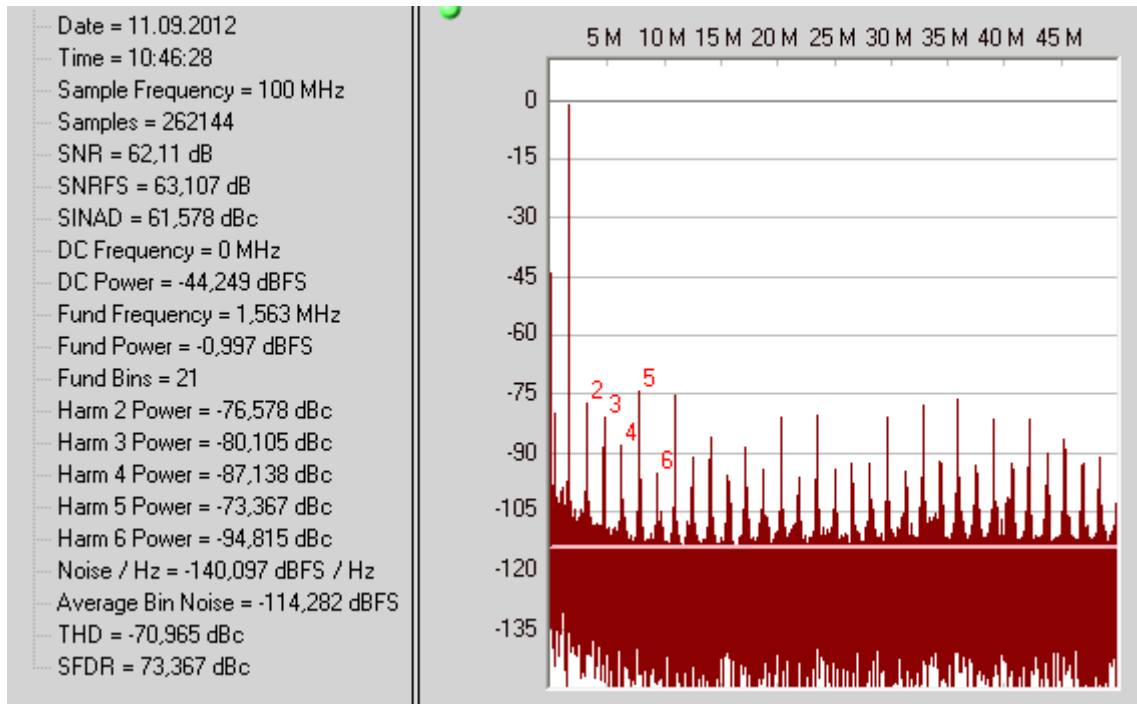


Figure 3: Single-Tone FFT with  $F_{IN} = 1.5625$  MHz,  $F_S = 100$  MSPS

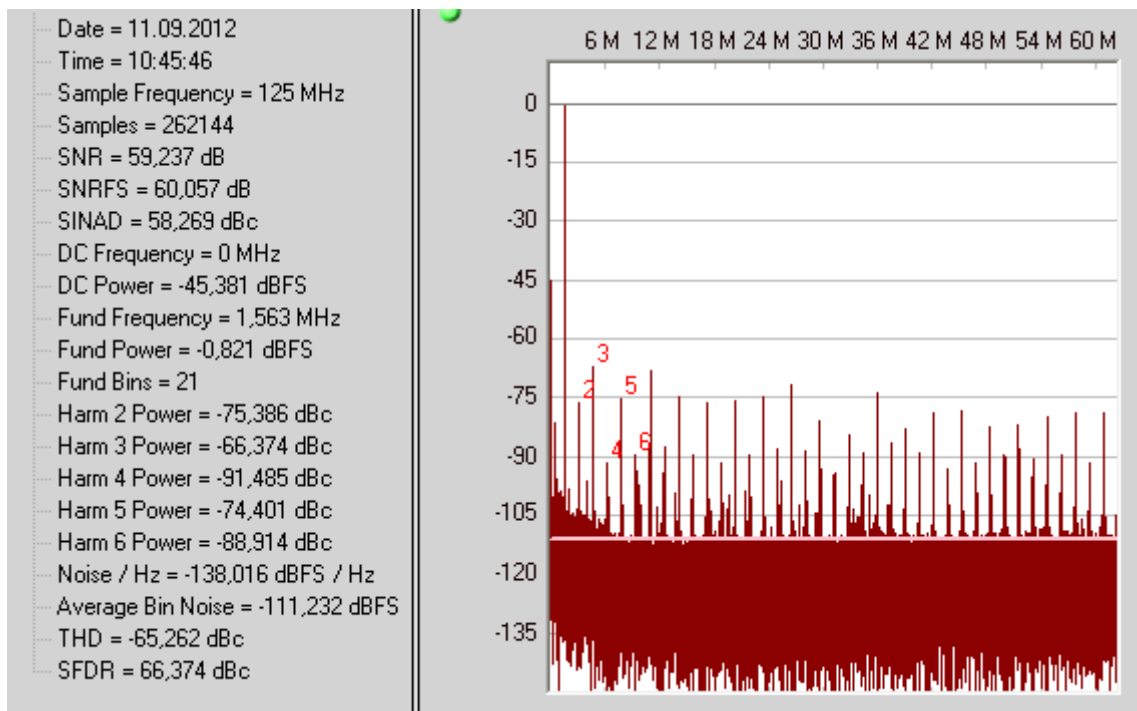


Figure 4: Single-Tone FFT with  $F_{IN} = 1.5625$  MHz,  $F_S = 125$  MSPS

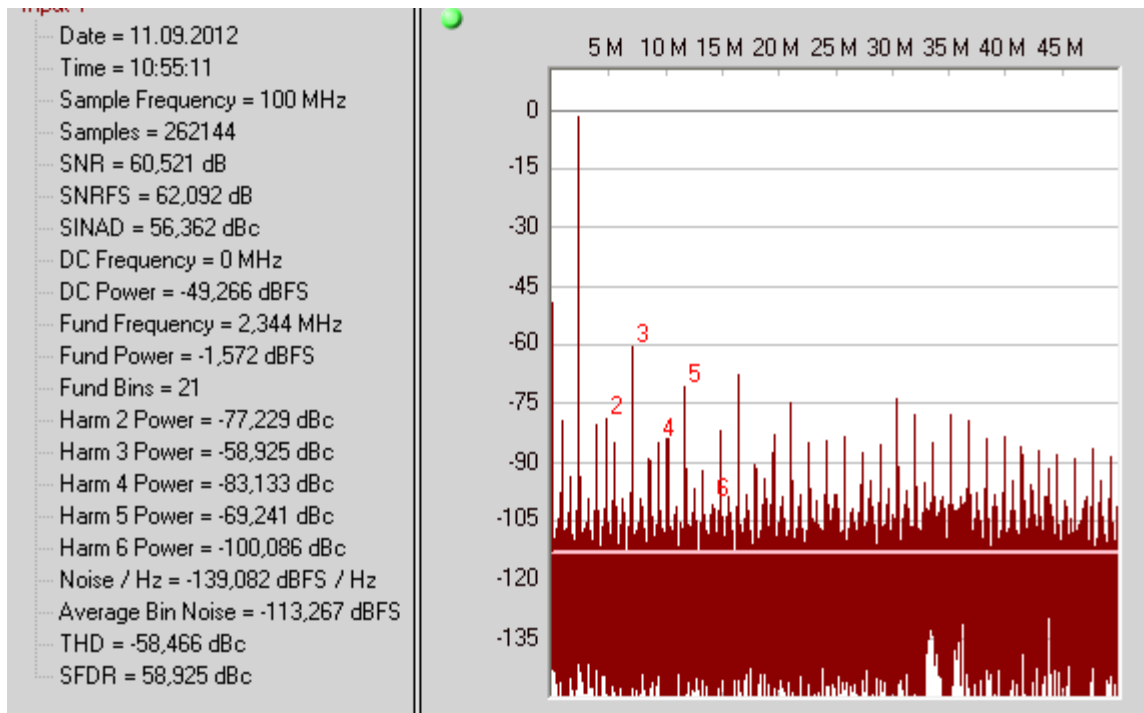


Figure 5: Single-Tone FFT with  $F_{IN} = 2.34375$  MHz,  $F_S = 100$  MSPS

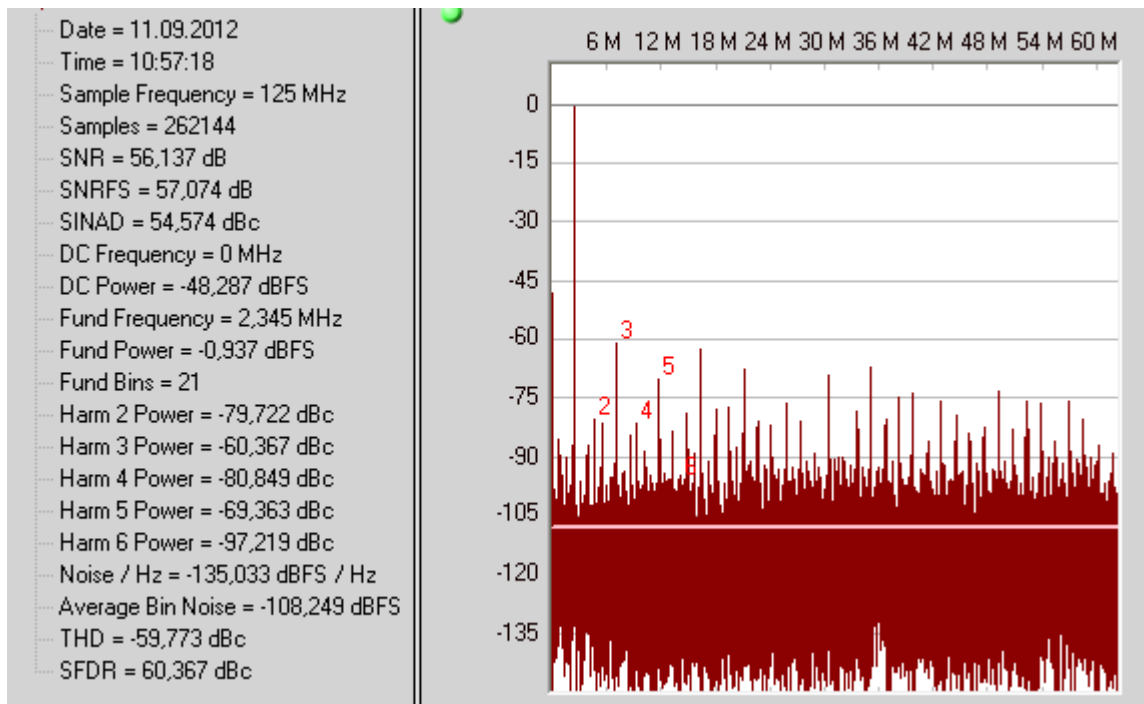


Figure 6: Single-Tone FFT with  $F_{IN} = 2.34375$  MHz,  $F_S = 125$  MSPS



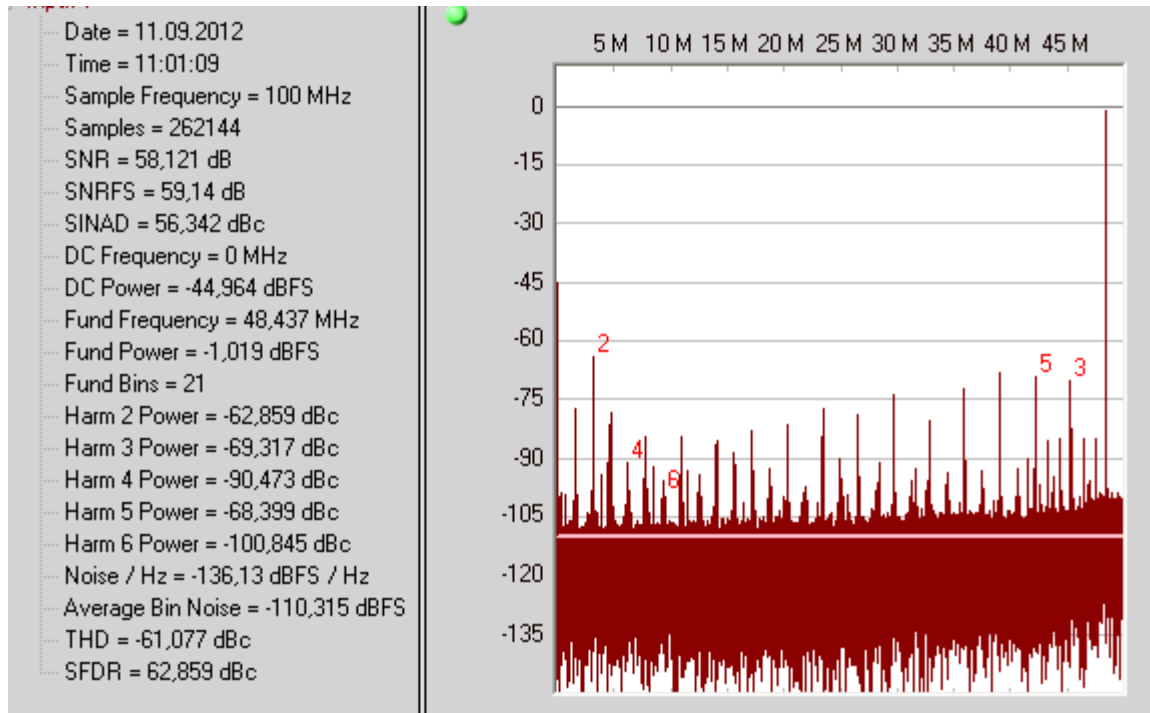


Figure 7: Single-Tone FFT with  $F_{IN} = 51.5625$  MHz,  $F_S = 100$  MSPS

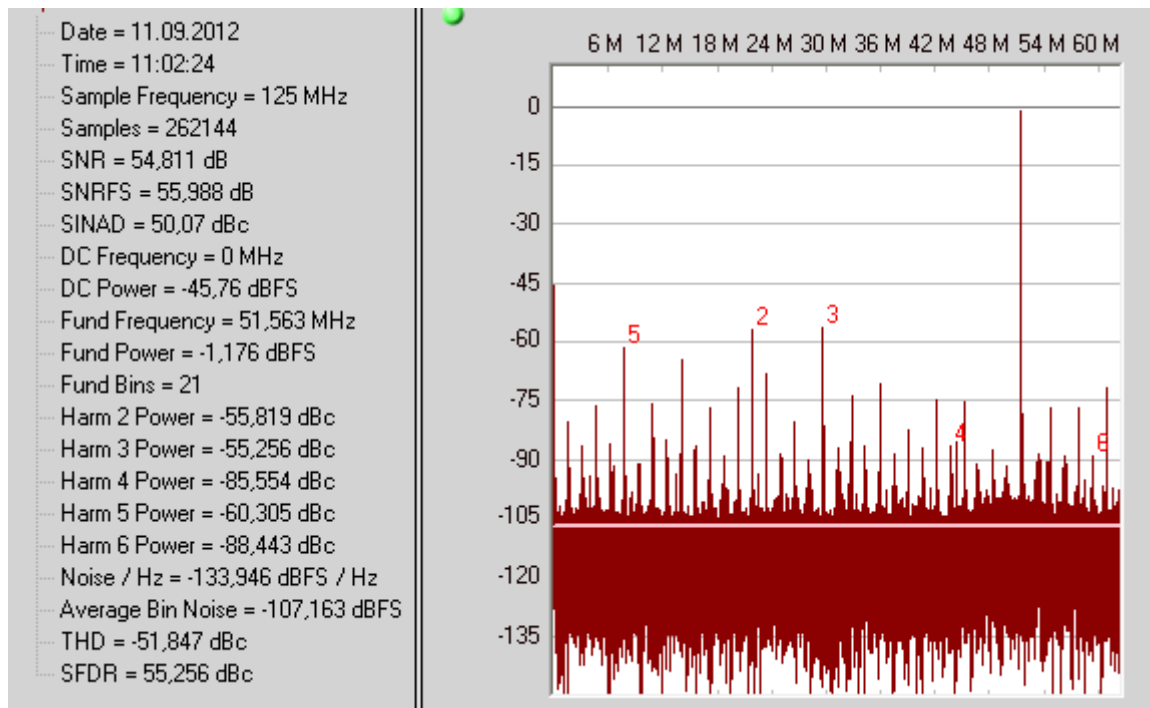


Figure 8: Single-Tone FFT with  $F_{IN} = 51.5625$  MHz,  $F_S = 125$  MSPS

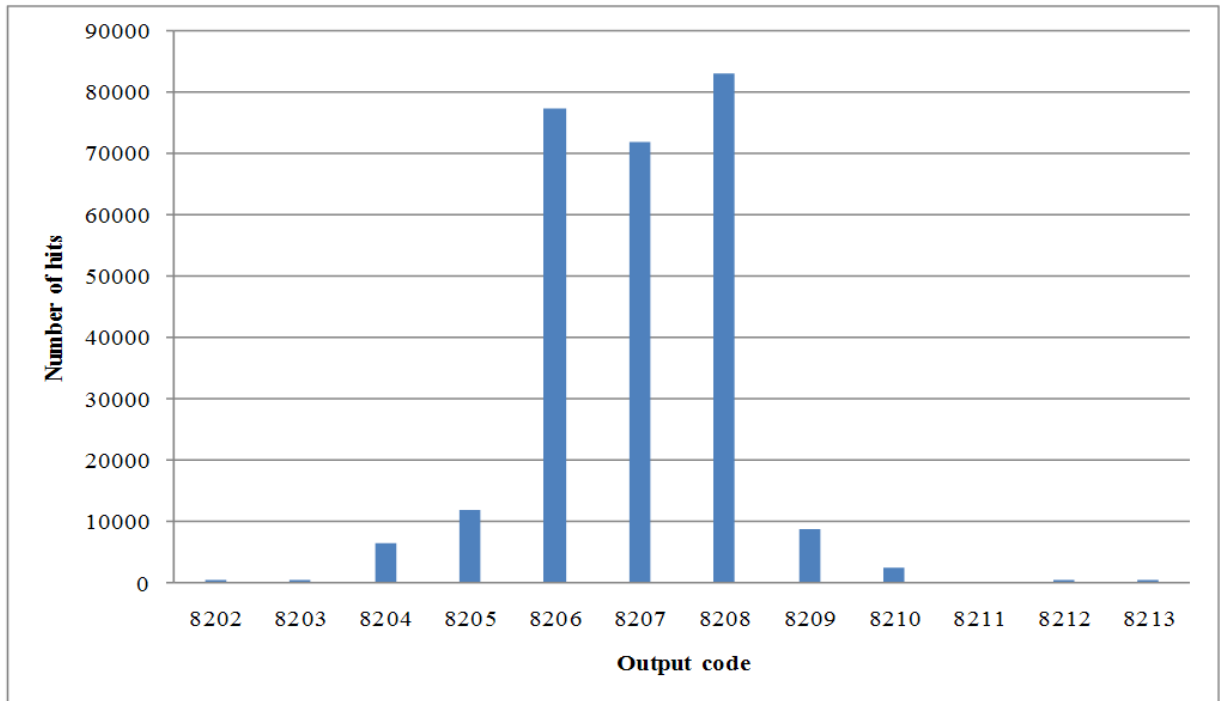


Figure 9: Shorted Input Histogram,  $F_s = 100$  MSPS

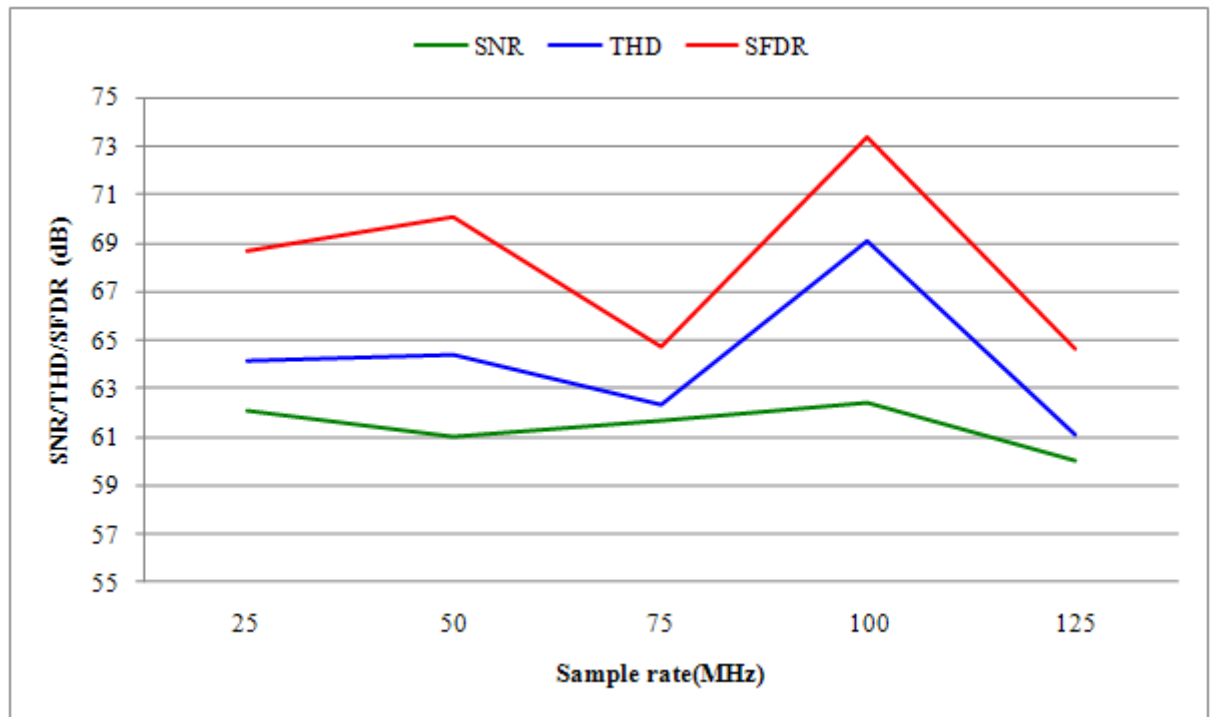


Figure 10: SNR/THD/SFDR vs.  $F_s$ ,  $F_{IN} = 1.5625$  MHz, -1 dB FS

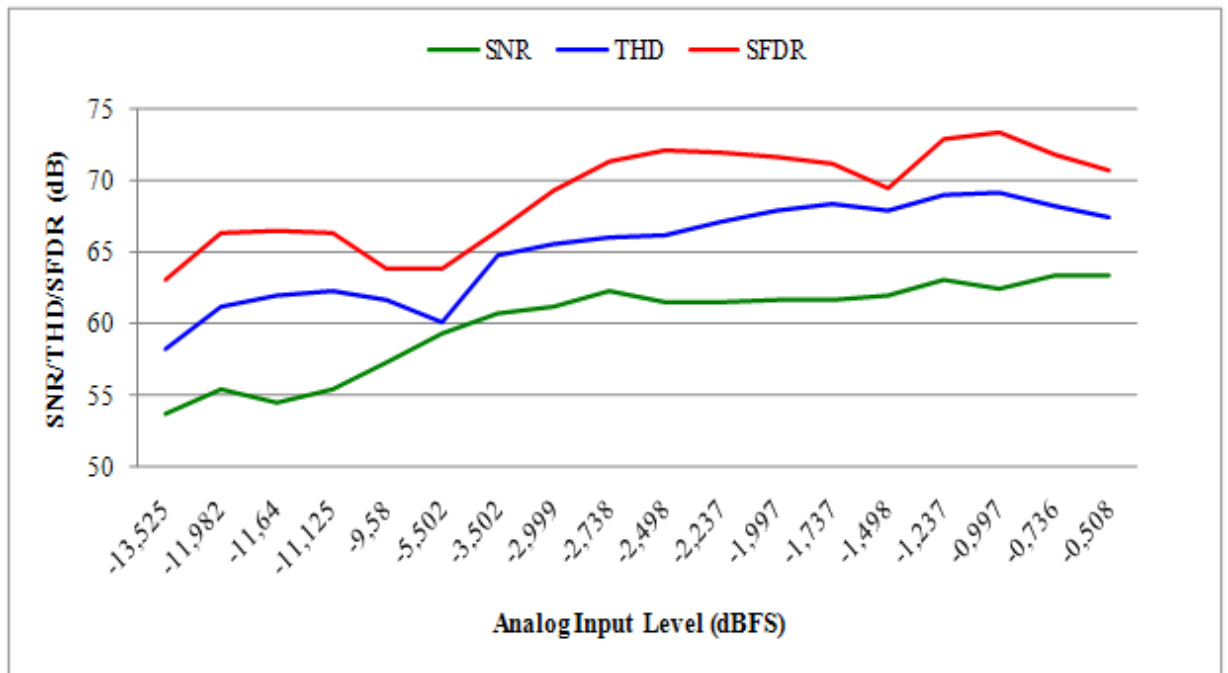


Figure 11: SNR/THD/SFDR vs. Analog Input Level,  $F_{IN} = 1.5625$  MHz,  $F_S = 100$  MSPS

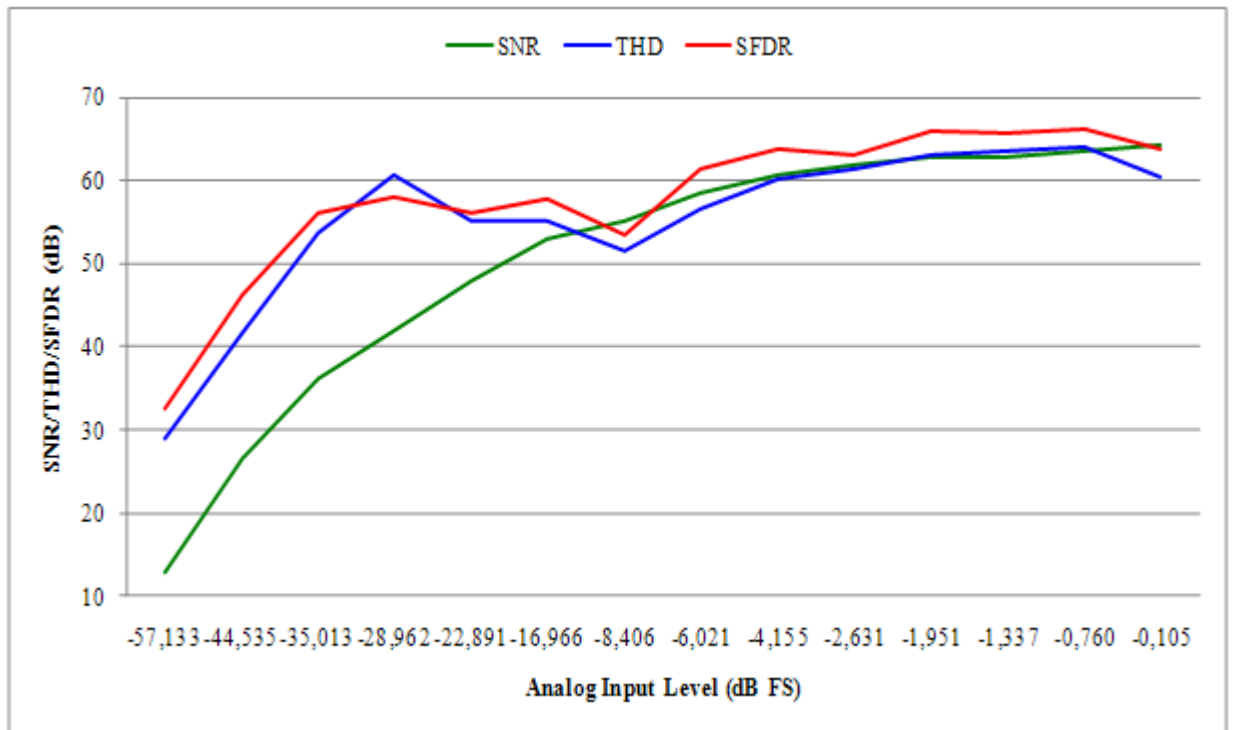


Figure 12: SNR/THD/SFDR vs. Analog Input Level,  $F_{IN} = 1.5625$  MHz,  $F_S = 100$  MSPS



Figure 13: SNR/THD/SFDR vs. Analog Input Level,  $F_{IN} = 1.5625$  MHz,  $F_S = 125$  MSPS

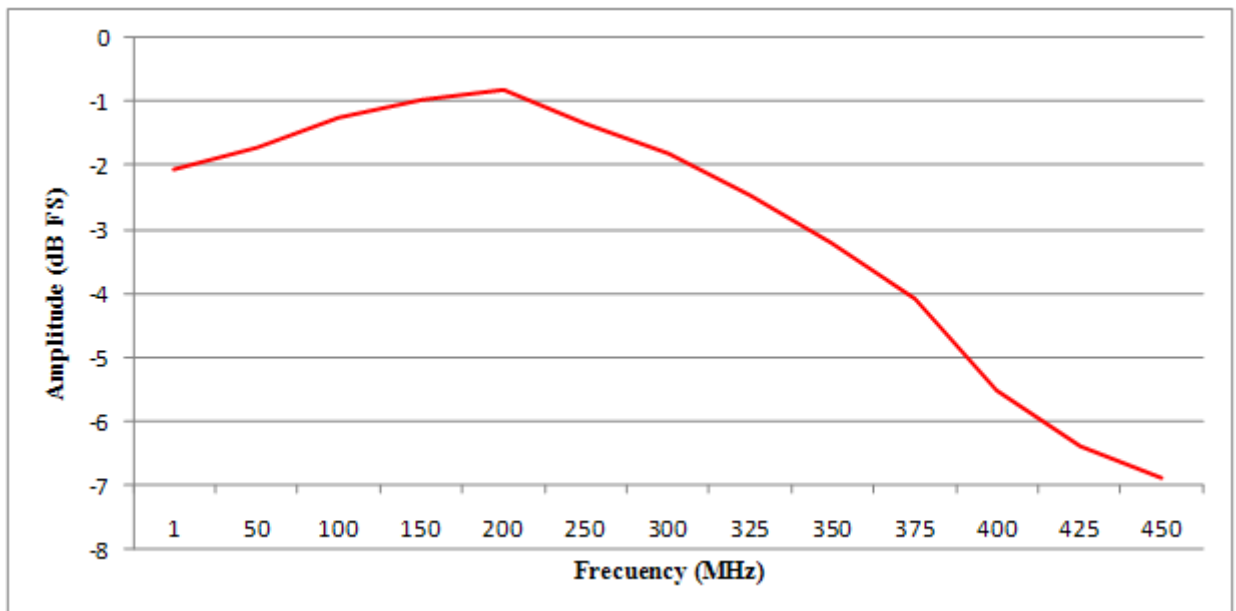


Figure 14: Full-Power vs. Frequency,  $F_S = 100$  MSPS

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## 9. DELIBERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation