14-bit 1-channel 50 MSPS pipeline ADC

SPECIFICATION

1 FEATURES

- TSMC MS CMOS 90nm
- Resolution 14-bit pipelined ADC
- Sampling 50 MSPS
- Different power supplies for digital (1 V and 1.8 V) and analog (1.8 V) parts
- Low standby current < 5uA
- Low power dissipation 171mW
- Spurious-free dynamic range 77dB
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Optical networking
- Test equipment
- Portable ultrasound and digital beam-forming systems
- Telecommunication systems
- High quality imaging video systems

3 OVERVIEW

The high-speed 14-bit ADC employs a high-performance differential pipeline architecture.
The ADC consists of a core ADC, LVDS clock receiver, output logic block, reference voltages and currents circuit. The output block aligns intermediate data at each stage, forms output code, and passes completed data to the output buffers.
The ADC requires 1.62 ÷ 1.98V analog supply and 0.9 ÷ 1.1V, 1.62 ÷ 1.98V digital supply voltages. This ADC supports standby mode which allows state with minimum power consumption. There is also the ability to configure the operating modes of the ADC with digital registers: register ref<3:0> controls the differential reference voltages, register ish<2:0> adjusts current of the sample and hold, register iadc<2:0> adjusts current of the core ADC.
The device is manufactured on TSMC MS CMOS 90nm technology.

4 STRUCTURE

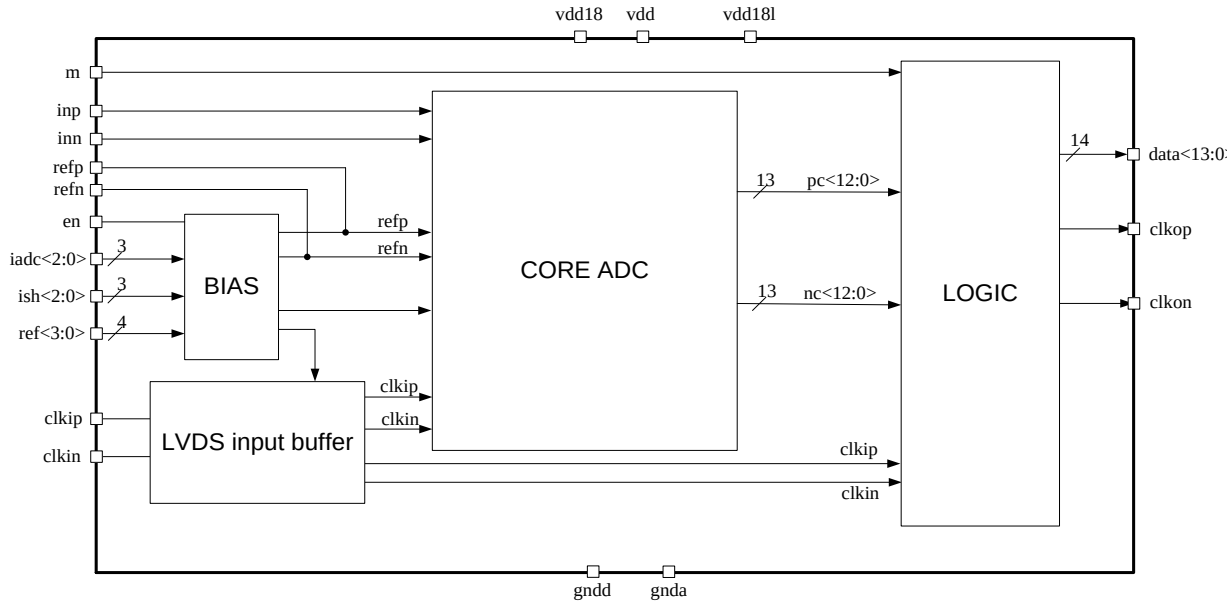

Figure 1: 14-bit 1-channel 50 MSPS pipeline ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
m	I	Output code type selection
inp	I	Differential analog input
inn	I	
en	I	Enable
iadc<2:0>	I	ADC Bias control
ish<2:0>	I	Sample-and-hold circuit bias control
ref<3:0>	I	Differential reference voltage control
clkip	I	Differential input clock
clkin	I	
data<13:0>	O	Output data
clkop	O	Differential clock output
clkon	O	
refp	I/O	Differential reference voltages
refn	I/O	
vdd18	I/O	Analog blocks supply voltage 1.8V
vdd18l	I/O	Digital blocks supply voltage 1.8V
vdd	I/O	Digital blocks supply voltage 1V
gnda	I/O	Analog blocks ground
gndd	I/O	Digital blocks ground

6 LAYOUT DESCRIPTION

Analog-to-digital converter layout dimensions are given in the table 1.

Table 1: Block dimensions of the 14-bit ADC

Dimension	Value	Unit
Height	1807	µm
Width	465	µm

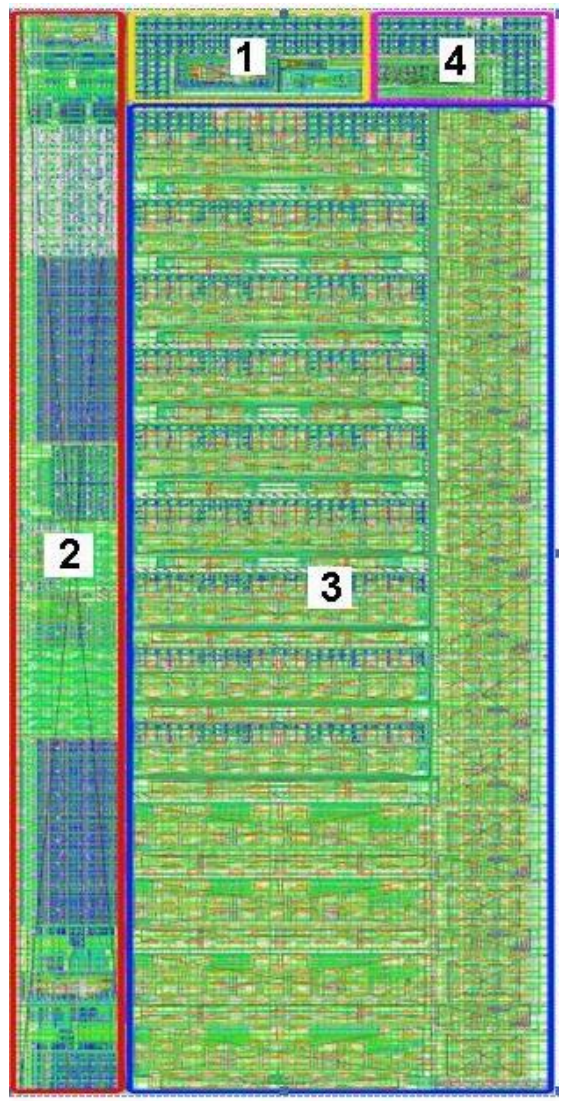

Figure 2: 14-bit ADC layout view

1. LVDS clock receiver
2. Currents and voltages reference
3. ADC core
4. Output logic

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC MS CMOS 90nm
Status silicon proven
Area 0.84 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd181}= V_{dd18} =1.62 ÷ 1.98 V,T = -40 ÷ +125°C, V_{dd}=0.9 ÷ 1.1V. Typical values are at V_{dd181} = V_{dd18} = 1.8V, V_{dd} = 1.0V, T = +27°C, unless otherwise noted.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Operating temperature range	T	-	-40	27	+125	°C
Analog blocks supply voltage	V_{dd18}	-	1.62	1.8	1.98	V
Digital blocks supply voltage	V_{dd18l}	-	1.62	1.8	1.98	V
Digital blocks supply voltage	V_{dd}	-	0.9	1	1.1	V
Resolution	N	-	-	14	-	bit
Sample rate	F_S	-	-	50	-	MSPS
Bandwidth	B	-	-	300	-	MHz
Current consumption	$I_{cnVdd18}$	V_{dd18}	82	90	97.5	mA
	$I_{cnVdd18l}$	V_{dd18l}	4.1	5	6	mA
	I_{cnVdd}	V_{dd}	-	100	-	µA
Standby current	I_{st}	-	-	5	-	µA
Reference voltages for the input signal	V_{REF+}	-	1.31	1.43	1.51	V
	V_{REF-}		0.37	0.41	0.44	V
Differential peak-to-peak input voltage range	$A_{IN\ d\ p-p}$	-	-	2	-	V
Input common mode voltage	U	-	$0.5V_{dd18}$ -100мВ	$0.5V_{dd18}$	$0.5V_{dd18}$ +100мВ	V
High level input voltage	V_{IH}	Digital inputs	0.7	-	-	V
Low level input voltage	V_{IL}		-	-	0.3	V

7.3 DYNAMIC CHARACTERISTICS

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Total Harmonic Distortion	THD	F_{IN} = 1.5625MHz F_{IN} = 2.34375MHz F_{IN} = 51.5625MHz	–	-76 -68 -58.9	-80	dB
Signal-to-Noise Ratio	SNR	F_{IN} = 1.5625MHz F_{IN} = 2.34375MHz F_{IN} = 51.5625MHz	–	64 62 52.8	67	dB
Spurious Free Dynamic Range	SFDR	F_{IN} = 1.5625MHz F_{IN} = 2.34375MHz F_{IN} = 51.5625MHz	–	77 68.1 59.9	82	dB
Signal-to-Noise And Distortion Ratio	SINAD	F_{IN} = 1.5625MHz F_{IN} = 2.34375MHz F_{IN} = 51.5625MHz	–	63.8 61 51.8	65	dB

8 TYPICAL CHARACTERISTICS

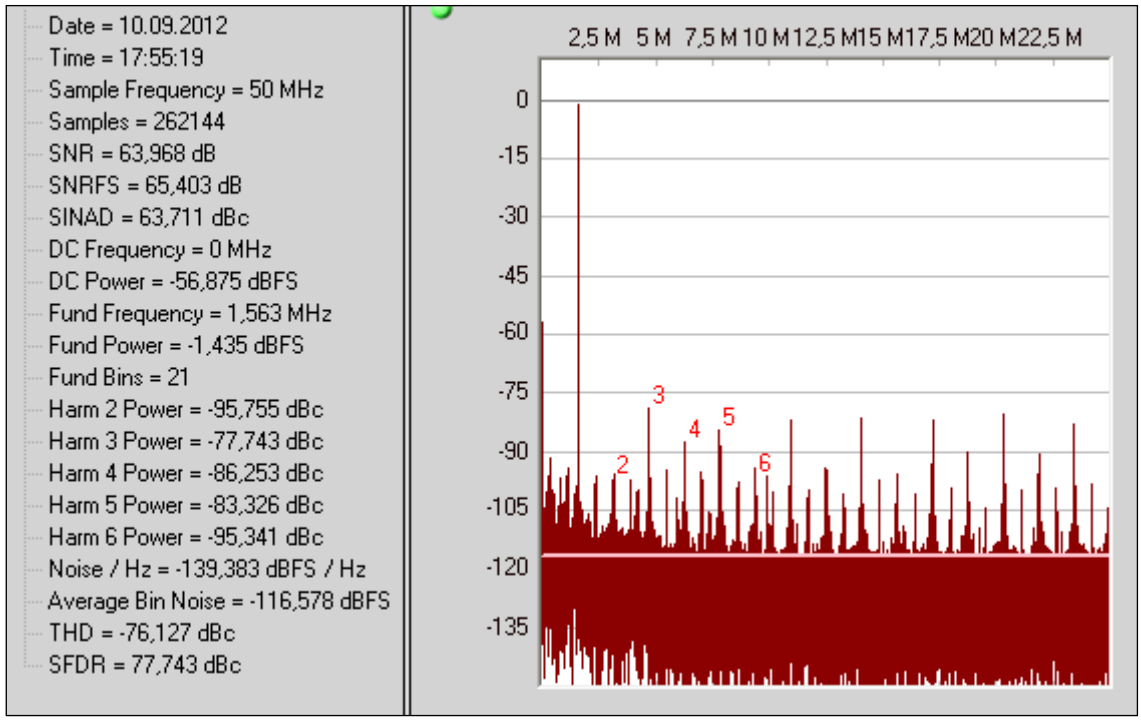

Figure 3: Single-Tone FFT with F_{IN} = 1.5625 MHz, F_S = 50 MSPS

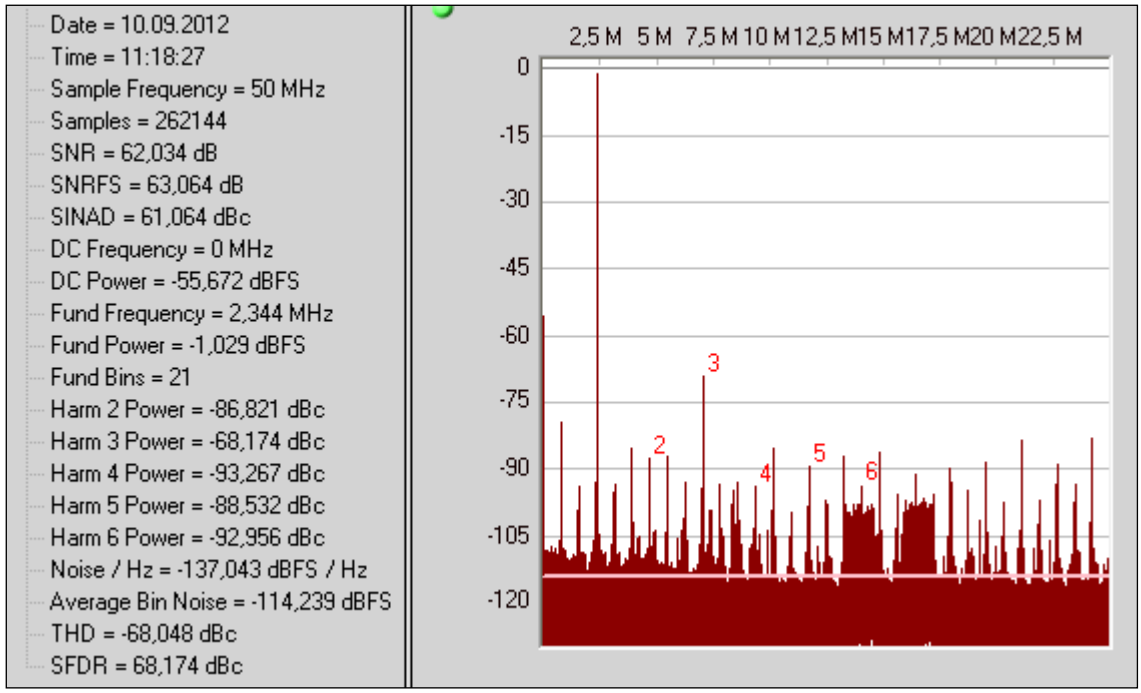

Figure 4: Single-Tone FFT with F_{IN} = 2.34375 MHz, F_S = 50 MSPS

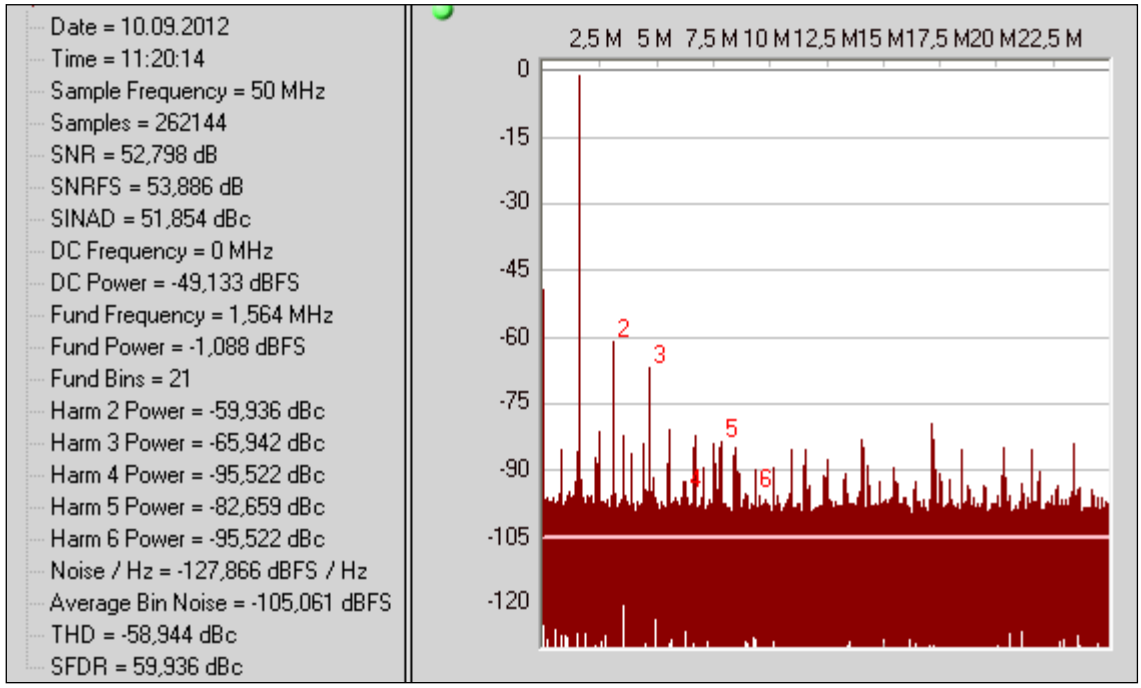

Figure 5: Single-Tone FFT with F_{IN} = 51.5625 MHz, F_S = 50 MSPS

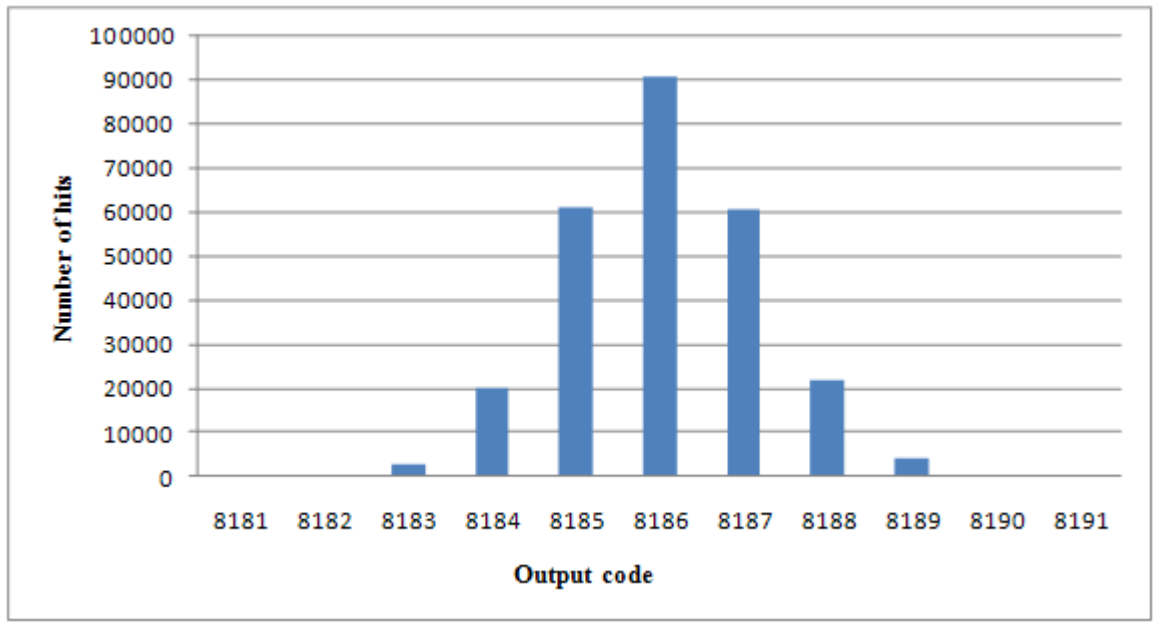

Figure 6: Shorted Input Histogram, F_S= 50 MSPS

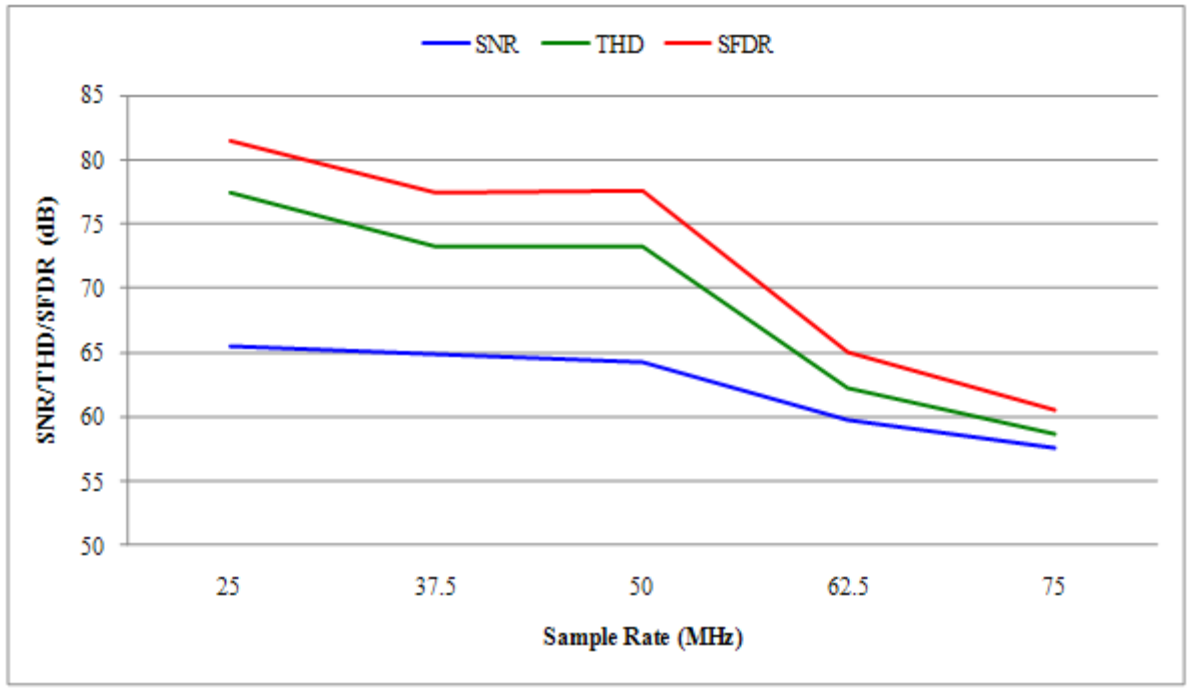

Figure 7: SNR/THD/SFDR vs. F_S, F_{IN} = 1.5625 MHz, -1 dB FS

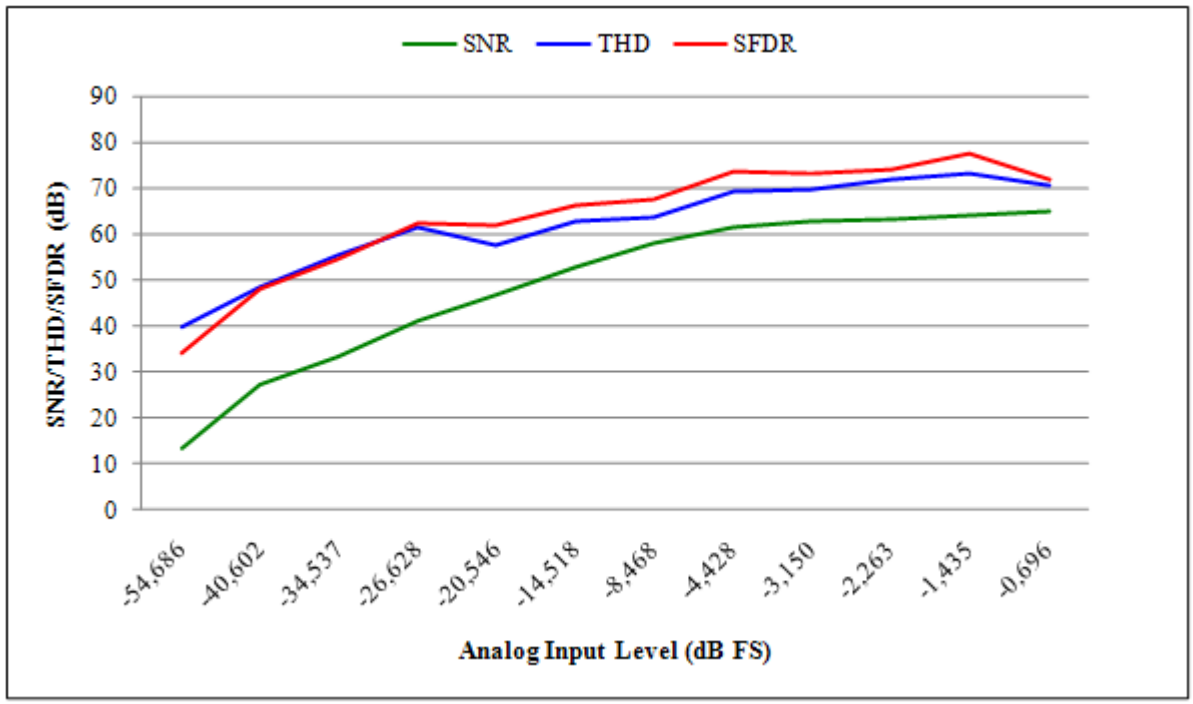

Figure 8: SNR/THD/SFDR vs. Analog Input Level, F_{IN} = 1.5625 MHz, F_S= 50 MSPS

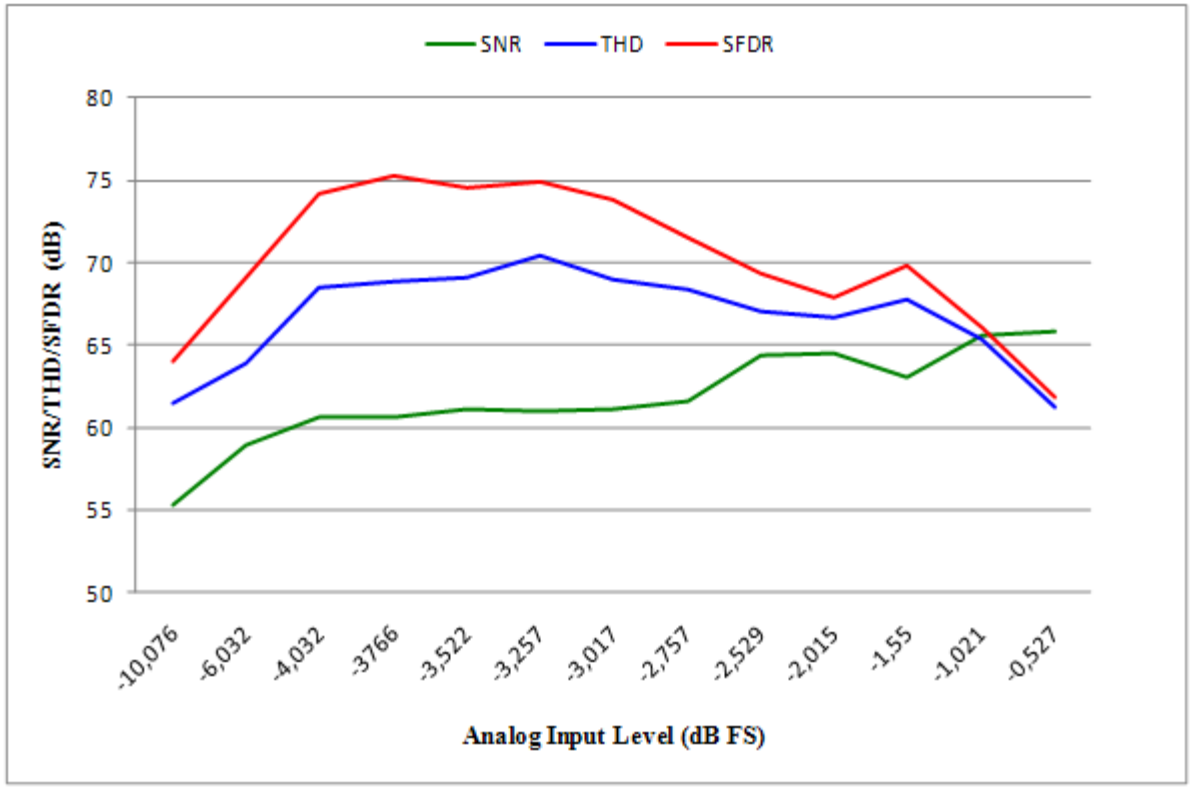

Figure 9: SNR/THD/SFDR vs. Analog Input Levels, F_{IN} = 1.5625 MHz, F_S= 50 MSPS

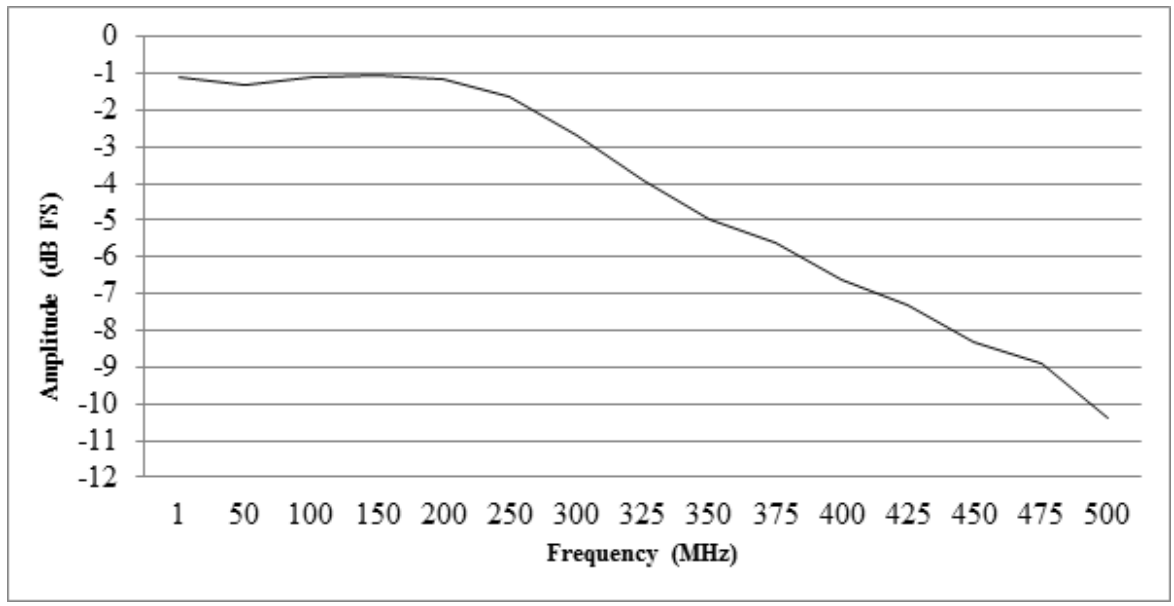

Figure 10: Full-Power vs. Frequency, F_S= 50 MSPS

9 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation