

## 12-bit 1-channel 1-10kSPS SAR ADC

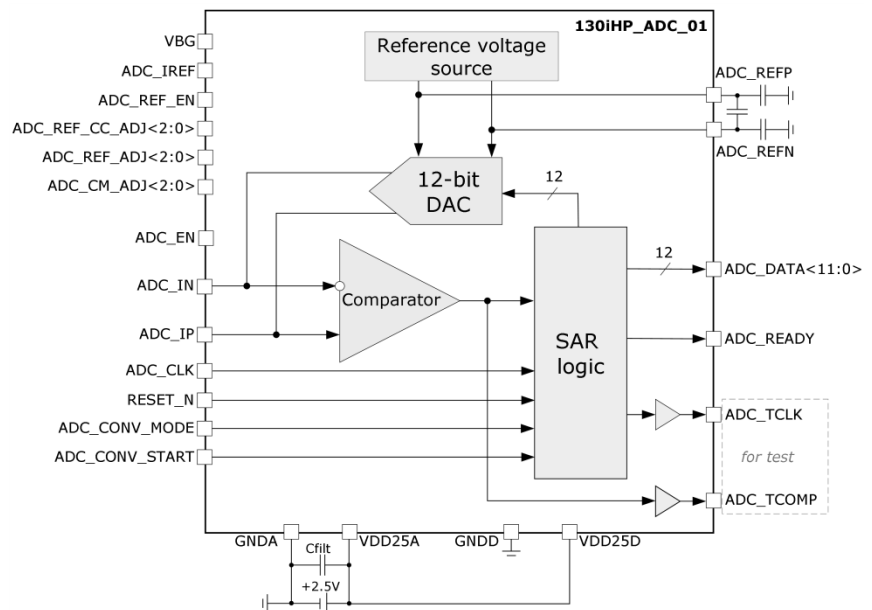
### OVERVIEW

130iHP\_ADC\_01 employs high-performance successive approximation architecture. The ADC operates with sampling rate from 1 to 10 kSPS and input clock from 14 to 140 kHz. The block has differential input and can operate in two modes: single measurement or continuous measurement. The ADC supports standby mode and features low power consumption, compact area.

IP technology: iHP SiGe BiCMOS 0.13um technology.

IP status: silicon proven.

Area: 0.43 mm<sup>2</sup>.



### ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V <sub>DD25A</sub>	-	2.4	2.5	2.6	V
	V <sub>DD25D</sub>	-	2.4	2.5	2.6	
Operating temperature range	T <sub>j</sub>	-	-40	+27	+85	°C
Clock frequency	F <sub>CLK</sub>	-	14	140	-	kHz
Sample rate	F <sub>S</sub>	-	1	10	-	kSPS
Resolution	N	-	-	12	-	bit
Effective number of bits	ENOB	F <sub>S</sub> =10kSPS	-	10	-	bit
Spurious-free dynamic range	SFDR	F <sub>S</sub> =10kSPS	-	64	-	dB
Differential nonlinearity	DNL	-	-	-	±1	LSB
Reference voltage	V <sub>REFP</sub>	-	-	1.75	-	V
	V <sub>REFN</sub>	-	-	0.75	-	
Power consumption	P <sub>TOTAL</sub>	Standby mode	-	0.5	-	uW
		Active mode @10kSPS	-	1	-	mW
Differential input voltage range	V <sub>IN p-p</sub>	Peak-to-peak differential	-	2	-	V
Clock duty cycle	S	Input clock signal	45	50	55	%
Input high-logic level	V <sub>IH</sub>	-	V <sub>DD25D</sub> -0.3	-	V <sub>DD25D</sub>	V
Input low-logic level	V <sub>IL</sub>	-	0	-	0.3	
Output high-logic level	V <sub>OH</sub>	-	V <sub>DD25D</sub> -0.3	-	V <sub>DD25D</sub>	V
Output low-logic level	V <sub>OL</sub>	-	0	-	0.3	