12-bit 2-channel 5 MSPS cascade delta-sigma ADC

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.13 um
- Switchable ENOB 8/10-bit accuracy
- Operational amplifiers' current adjustment
- Supply voltage - 3.3 V
- Input differential signal range - 2 V
- Clock frequency divider
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, Vanguard, SilTerra

2 APPLICATION

- Analog to digital conversion of wide-band signal
- Receivers, transceivers
- Analog integral circuits
- Measurement environment
- Medicine environment

3 OVERVIEW

The block is third order cascade (2-1) delta-sigma ADC with 5-level quantizer in both stages. The block consists of:

- Two delta-sigma modulators second and first order, coupled in series and combined by noise cancellation logic
- Clock splitter
- Block of bias currents, tunable (3-bit control)
- Block of reference voltages, tunable (5-bit control)
- Clock frequency divider (4-bit control)
- DWA-correction of capacitors' mismatch

Output signal is represented in thermometer code at the output of each stage. There is a possibility to disable the second stage of modulator to save the power with decreased accuracy. Next to options included: DWA correction algorithm; tuning of reference voltages buffers; tuning of bias current for operational amplifiers with 3-bit control; the clock frequency divider with integer ratio 1-15. Input signal common mode voltage is 1.65 V; recommended values of reference voltages: 0.9 ± 0.4 V; recommended differential input signal amplitude - 0.64 V p-p; allowable duty cycle: 50 ± 5%.
The block is designed on iHP SiGe BiCMOS 0.13 um technology.

4 STRUCTURE

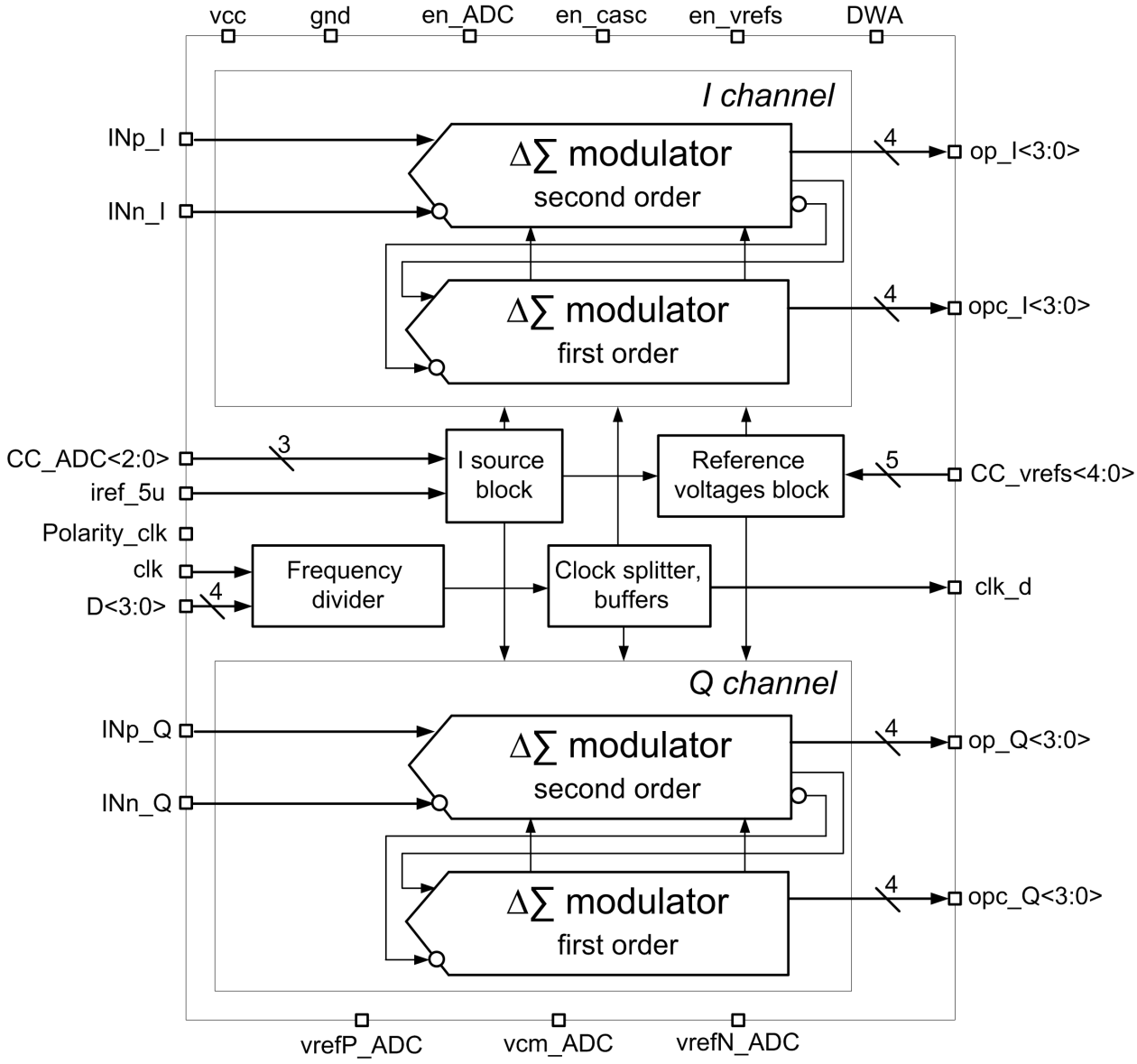

Figure 1: ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
iref_5u	I	Reference current 5 uA (influent)
clk	I	Clock signal
INp_I	I	Input differential signal, I channel
INn_I		
INp_Q	I	Input differential signal, Q channel
INn_Q		
D<3:0>	I	Frequency division coefficient
Polarity_clk	I	Polarity switch of clock signal
en_ADC	I	ADC enable
en_casc	I	ADC enable second cascade
en_vrefs	I	Block of reference voltages enable
DWA	I	DWA enable
CC_ADC<2:0>	I	Opamps current control
CC_vrefs<4:0>	I	Voltage buffers current control
op_I<3:0>	O	I channel ADC main cascade digital output data
opc_I<3:0>	O	I channel ADC second cascade digital output data
op_Q<3:0>	O	Q channel ADC main cascade digital output data
opc_Q<3:0>	O	Q channel ADC second cascade digital output data
clk_d	O	Output clock signal
vrefP_ADC	IO	Differential reference voltage
vrefN_ADC		
vcm_ADC	IO	Common mode voltage
vcc	IO	Supply voltage 3.3 V
gnd	IO	Ground voltage

6 LAYOUT DESCRIPTION

The ADC dimensions are given in the table 2.

Table 2: Block dimensions

Dimension	Value	Unit
Height	650	um
Width	350	um

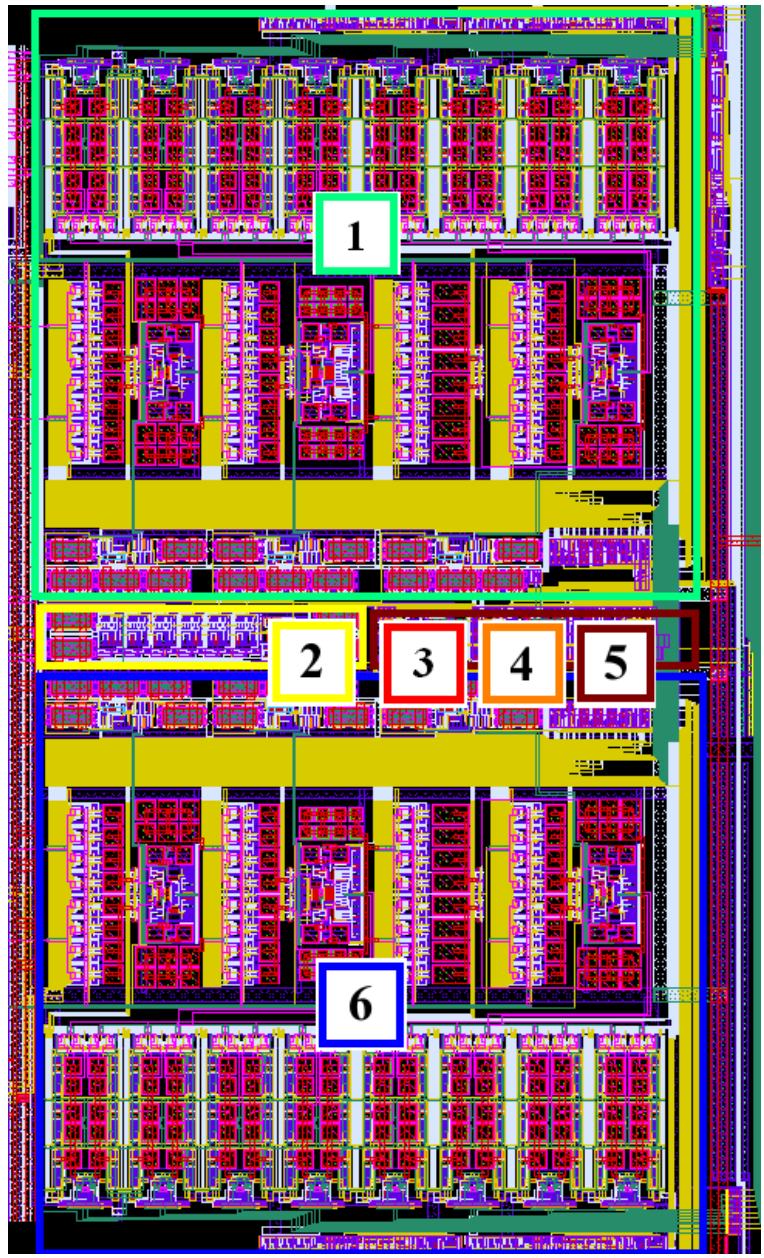

Figure 2: ADC layout

1. DSM, I channel
2. Current source
3. Frequency diviver
4. Reference voltage block
5. Clock splitter + buffers
6. DSM, Q channel

The reference voltages block is built as separated component to simplify the total layout design. The block consists of three voltages buffers and the control circuit. The height of one buffer is 62 um, the width is 167 um. The layout view of one of the buffers is shown in figure 3.

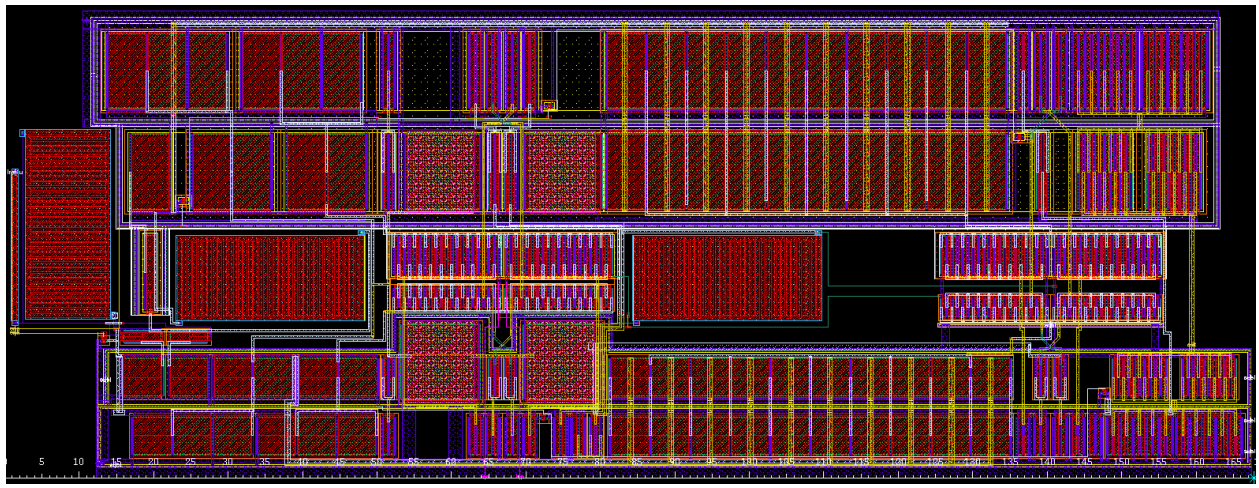

Figure 3: The voltage buffer layout

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.13 um
Status _____ silicon proven
Area _____ 0.23 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical parameters are given for V_{CC} = 2.7 ÷ 3.6 V and T_j= -40 ÷ +85°C, unless otherwise specified; typical values are given for V_{CC} = 3.3 V and T_j = 27° C.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Operating temperature	T_j	-	-40	27	+85	°C
Supply voltage	V_{CC}	-	2.7	3.3	3.6	V
Reference voltage	V_{ref}	-	0.5	0.9	1.3	V
Resolution	N	-	-	12	-	bit
Signal to noise ratio	SNR	Band 150 kHz	47	-	62	dB
Spurious-free dynamic range	SFDR	-	60	-	70	dB
Oversampling ratio	OSR	-	-	16	-	-
Bandwidth	BW	-	150	-	230	kHz
Sampling rate	F_s	-	5	-	7.5	MSPS
Duty cycle	S	-	45	50	55	%
Standby power	P_{st}	-	0.18	1.08	3.43	uW
Effective number of bits	ENOB	Fin = 40 kHz, Fclk = 5 MHz, Vin (dif p-p) = 1.6 V, (schematic, 2nd cascade off)	-	9.07	-	bit
		Fin = 40 kHz, Fclk = 5 MHz, Vin (dif p-p) = 1.6 V, (schematic, 2nd cascade on)	-	11.29	-	
		Fin = 40 kHz, Fclk = 5 MHz, Vin (dif p-p) = 1.6 V, (parasitic extraction, 2nd cascade off)	-	8.31	-	
		Fin = 40 kHz, Fclk = 5 MHz, Vin (dif p-p) = 1.6 V, (parasitic extraction, 2nd cascade on)	-	10.09	-	
		Fin = 80 kHz, Fclk = 5 MHz, Vin (dif p-p) = 1 V, (parasitic extraction, 2nd cascade off)	-	7.62	-	
		Fin = 80 kHz, Fclk = 5 MHz, Vin (dif p-p) = 1 V, (parasitic extraction, 2nd cascade on)	-	9.2	-	
Total power	P_{supply}	Both channels with second cascade on	2.99	4.62	5.29	mW
		Both channels with second cascade off	2.67	3.70	4.43	mW
Differential input voltage range	$A_{IN\ p-p}$	-	-	0.64	-	V p-p
Voltage reference supply current	I_{VREFS}	-	0.59	0.64	0.64	mA
Supply current (one channel)	I_{ADC}	With second cascade on	0.21	0.34	0.36	mA
		With second cascade off	0.17	0.25	0.26	mA

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Total supply current	I_{supply}	Both channels with second cascade on	1.11	1.40	1.47	mA
		Both channels with second cascade off	0.99	1.12	1.23	mA
Common mode voltage	U	-	-	1.65	-	V
Input high-logic level	V_{IH}	For digital inputs	$0.7V_{CC}$	-	$V_{CC}+0.25$	V
Input low-logic level	V_{IL}		-0.25	-	$0.3V_{CC}$	V

8 DYNAMICAL CHARACTERISTICS

The results of testing of ADC schematics are shown in figure 4 and figure 5.

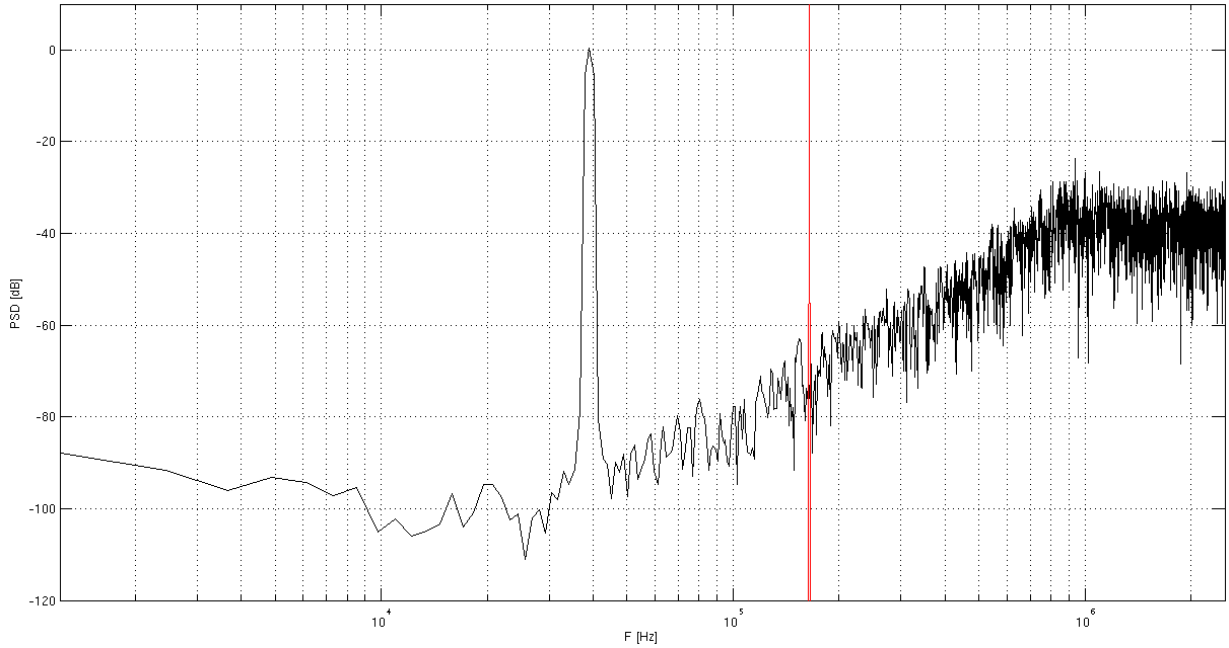

Figure 4: Output signal spectra (second cascade off)
Conditions: Fin = 40 kHz, Fclk = 5 MHz, Vin (dif p-p) = 1.6 V.
SNR = 56.38 dB, ENOB = 9.07 bit

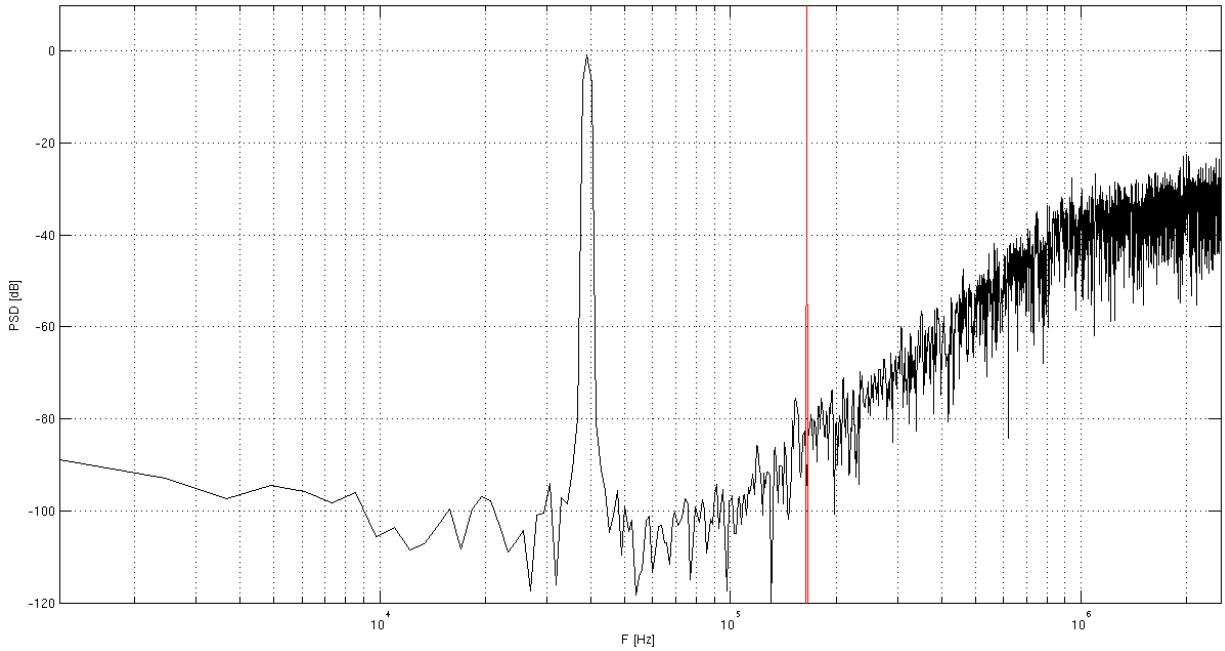

Figure 5: Output signal spectra (second cascade on)
Conditions: Fin = 40 kHz, Fclk = 5 MHz, Vin (dif p-p) = 1.6 V.
SNR = 69.71 dB, ENOB = 11.29 bit

The results of testing of ADC extraction view (both channels of ADC and reference voltages) are shown in figures 6 - 9.

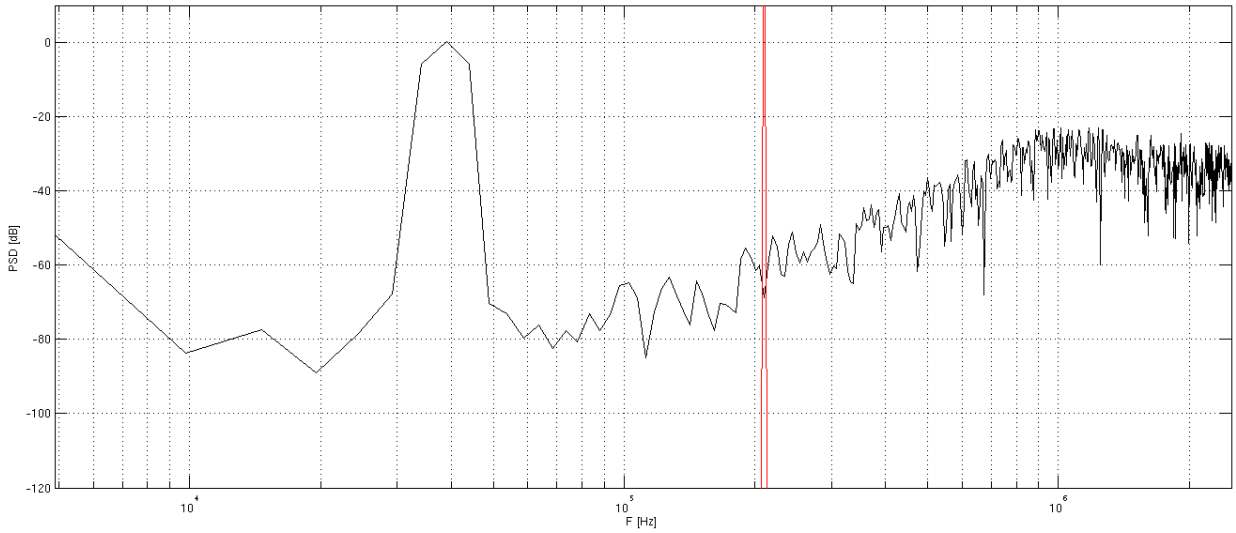

Figure 6: Output signal spectra (second cascade off). I channel
Conditions: Fin = 40 kHz, Fclk = 5 MHz, Vin (dif p-p) = 1.6 V.
SNR = 51.81 dB, ENOB = 8.31 bit

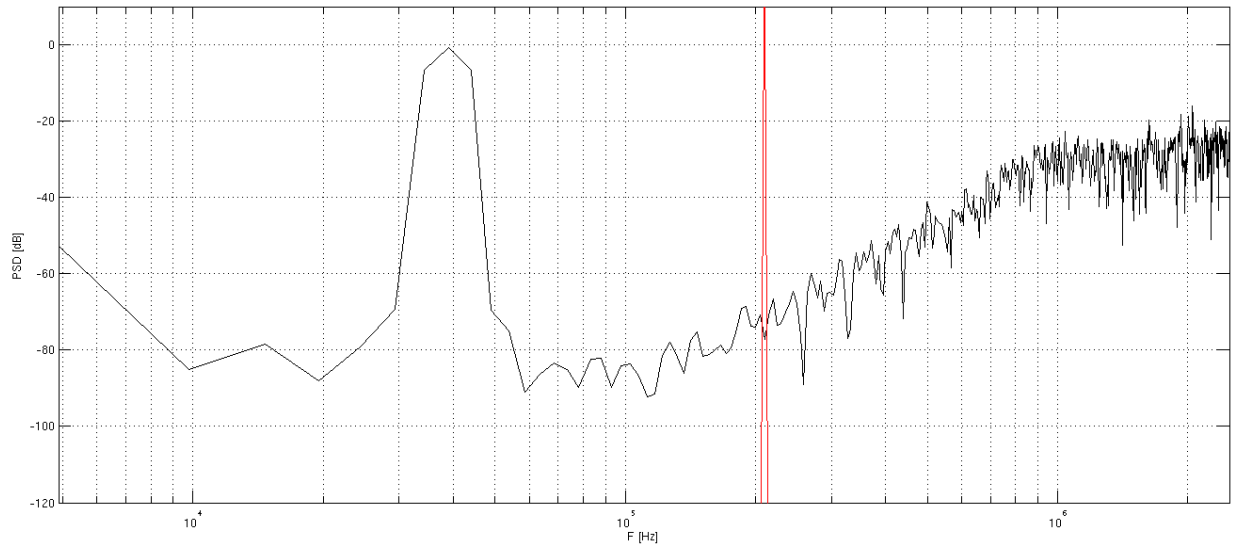

Figure 7: Output signal spectra (second cascade on). I channel.
Conditions: Fin = 40 kHz, Fclk = 5 MHz, Vin (dif p-p) = 1.6 V.
SNR = 62.51 dB, ENOB = 10.09 bit

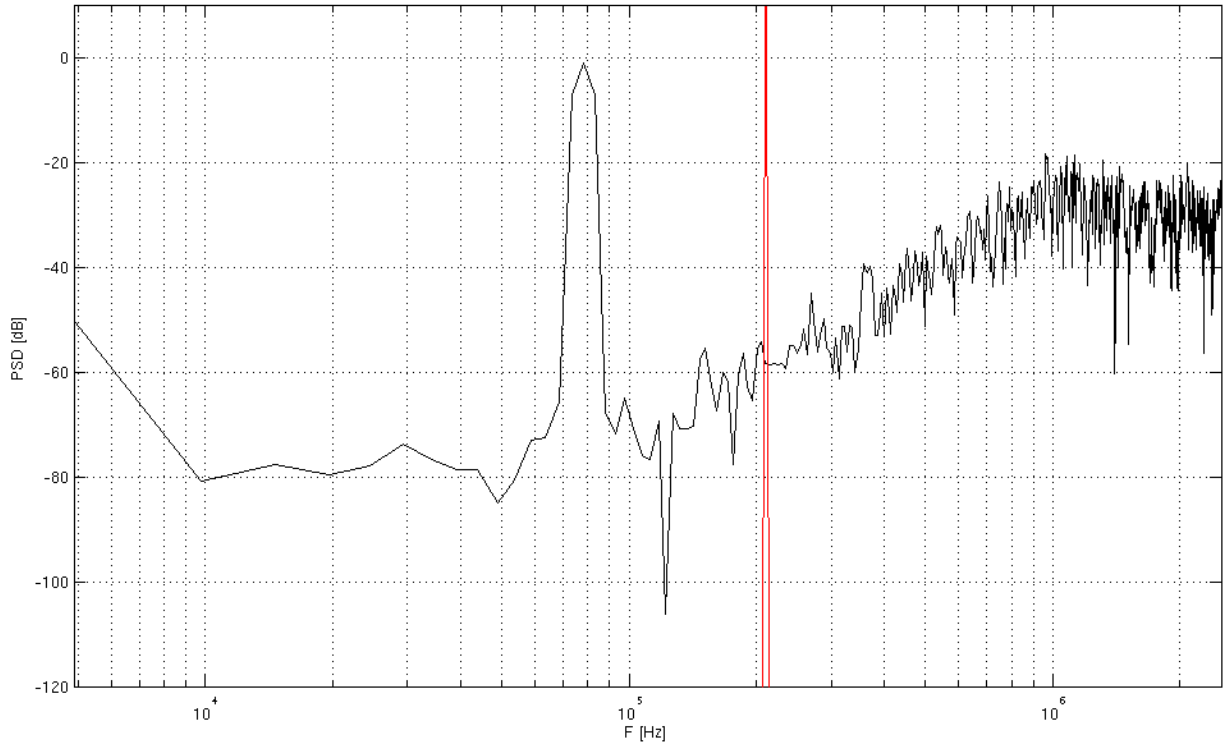

Figure 8: Output signal spectra (second cascade off). Q channel
Conditions: Fin = 80 kHz, Fclk = 5 MHz, Vin (dif p-p) = 1 V.
SNR = 47.62 dB, ENOB = 7.62 bit

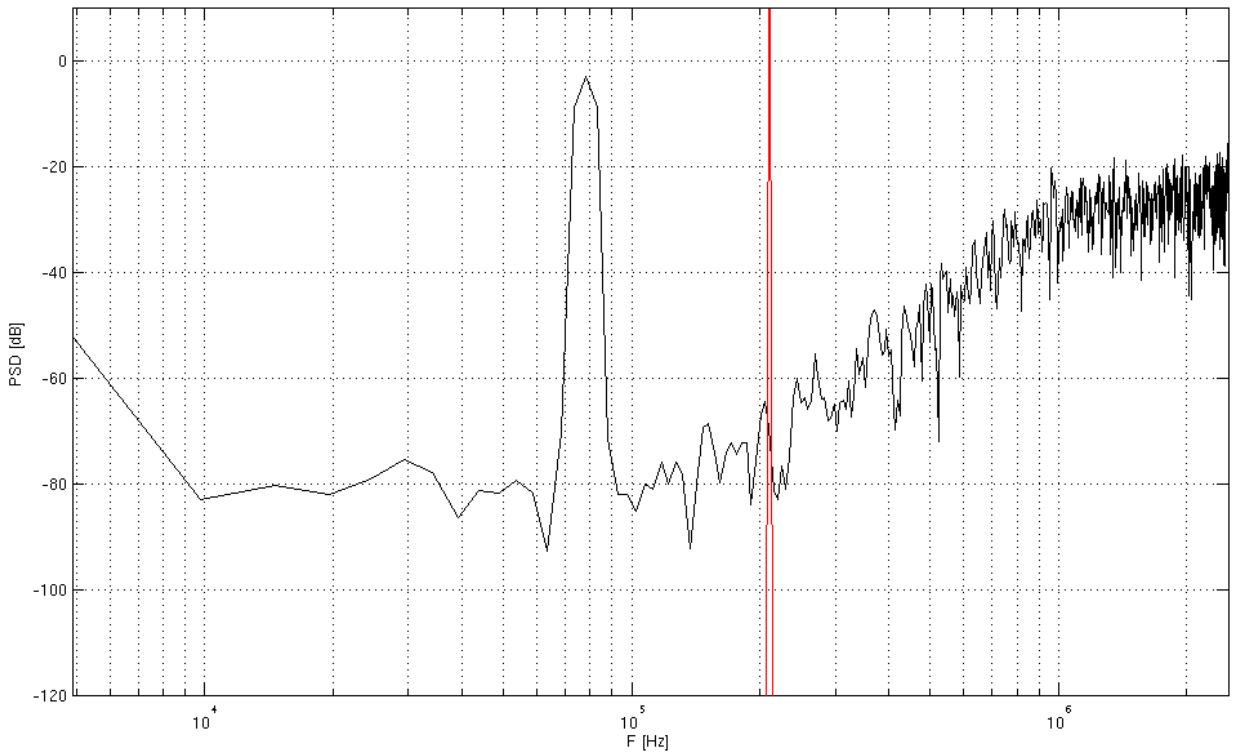

Figure 9: Output signal spectra (second cascade on). Q channel
Conditions: Fin = 80 kHz, Fclk = 5 MHz, Vin (dif p-p) = 1 V.
SNR = 57.14 dB, ENOB = 9.2 bit

9 DELIVERABLES

Depending on license type, IP may include:

- Schematic or NetList
- Layout or blackbox
- Verilog, lef and lib files
- Extracted view (optional)
- HDL-description of digital filters
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.0:

- Section 1 updated (refer to page 1)
- Section 4 updated (refer to page 2)
- Subsection 7.1 updated (refer to page 6)
- Subsection 7.2 updated (refer to page 6)

From version 1.1:

- Subsection 7.2 updated (refer to page 6)