12-bit 800 kSPS cascade delta-sigma ADC

SPECIFICATION

1 FEATURES

- TSMC BiCMOS SiGe 180 nm
- Resolution 12 bit
- Operational amplifiers' current adjustment
- Supply voltage - 1.8 V
- Input signal range 1.6 V (differential peak-to-peak)
- Built-in input signal level detection, sign detection
- Supported foundries: UMC, Global Foundries, SMIC, iHP, Vanguard, SilTerra

2 APPLICATION

- Analog to digital conversion of wide-band signal
- Receivers, transceivers
- Analog integral circuits
- Measurement environment
- Medicine environment

3 OVERVIEW

The block is third order cascade (2-1) delta-sigma ADC with 5-level quantizers in both stages. The block consists of:

- Two delta-sigma modulators second and first order, coupled in series and combined by noise cancellation logic
- Clock splitter
- Block of bias currents, tunable (3-bit control)
- DWA-correction of capacitors' mismatch
- Input signal level detection

Output signal is represented in thermometer code at the output of each stage. There is a possibility to disable the second stage of modulator, DWA correction. Tuning of bias current for operational amplifiers with 3-bit control included.
Common mode voltage - 0.9 V; recommended values of reference voltages: 0.9 ± 0.4 V; recommended differential input signal amplitude - 0.64 V; allowable duty cycle: 50 ± 5%.
The block is designed on TSMC BiCMOS SiGe 180 nm technology.

4 STRUCTURE

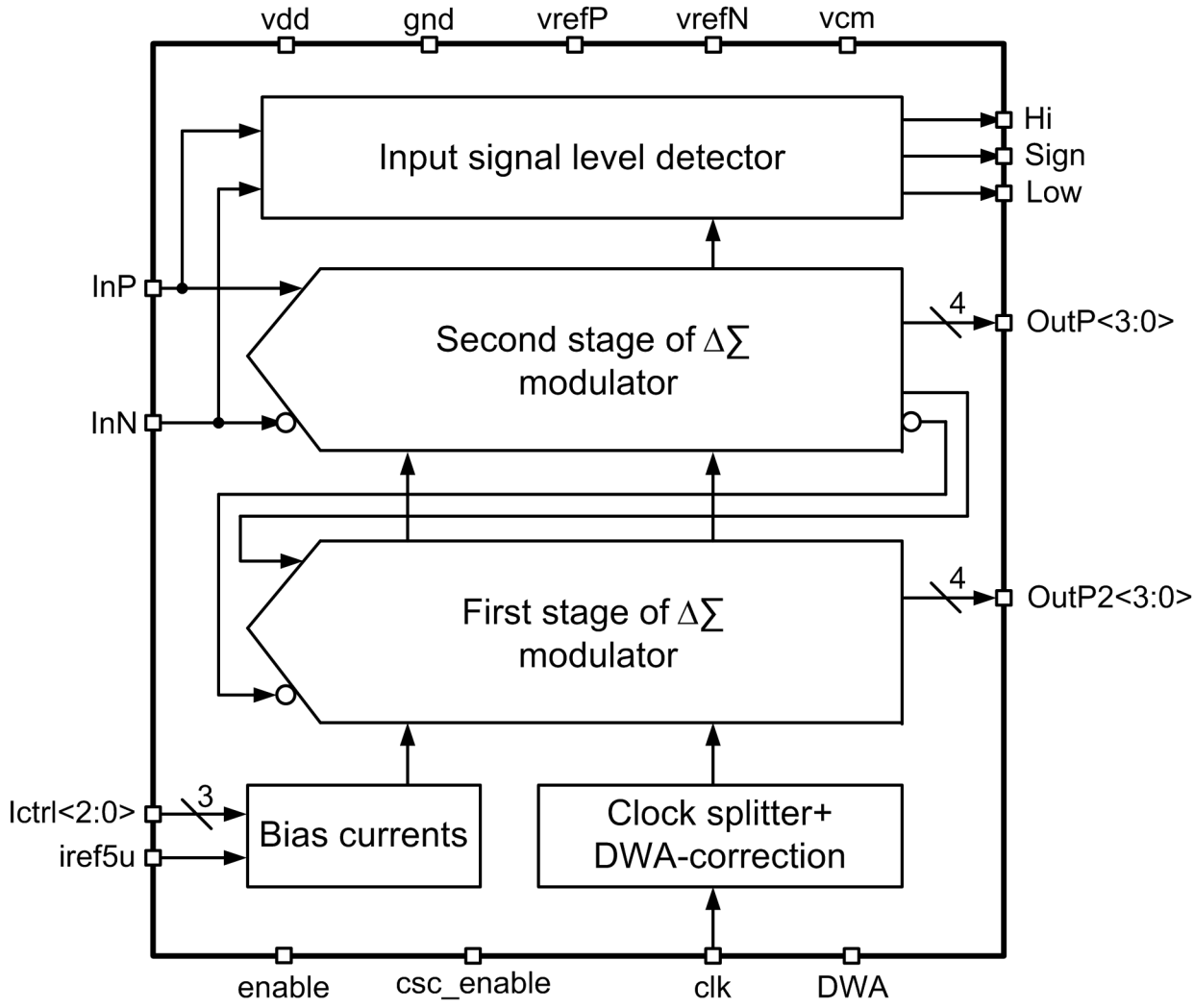

Figure 1: 12-bit cascade delta-sigma ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
iref5u	I	Reference current 5 uA (influent)
clk	I	Input clock
vrefP vrefN	I	Differential reference voltage
vcm	I	Common mode voltage
InP InN	I	Differential analog input signal
enable	I	General enable
csc_enable	I	Second stage modulator enable
DWA	I	DWA enable
Hi	O	Excess level signal
Low	O	Detraction level signal
Sign	O	Sign signal
Ictrl<2:0>	I	Tune of opamps current
OutP<3:0>	O	First stage modulator's output
OutP2<3:0>	O	Second stage modulator's output
vdd	IO	Supply voltage 1.8 V
gnd	IO	Ground

6 LAYOUT DESRIPTION

The block dimensions are given in table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	355	um
Width	406	um

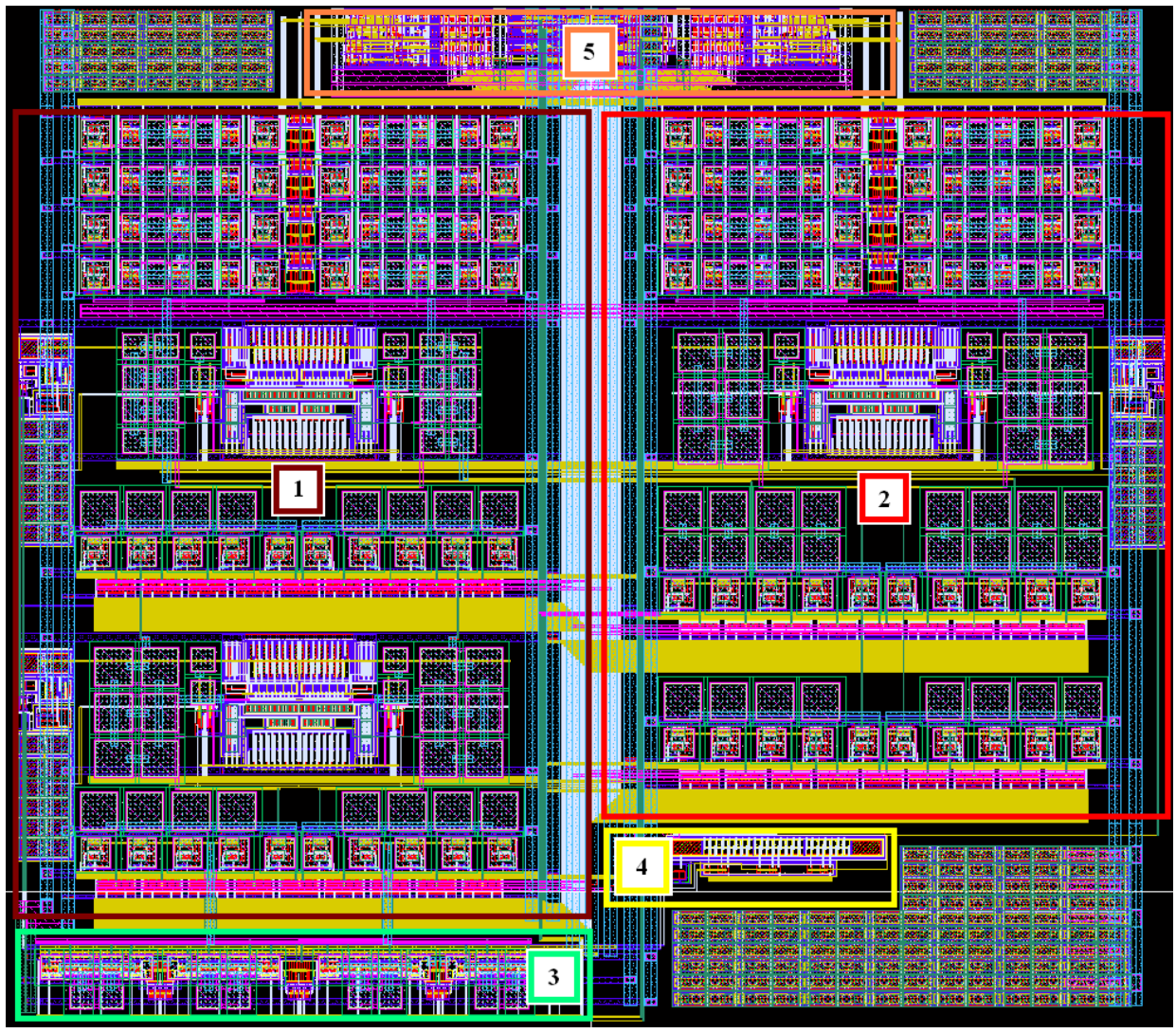

Figure 2: Layout 12-bitcascade delta-sigma ADC

1. First stage of delta-sigma modulator
2. Second stage of delta-sigma modulator
3. Input signal level detector
4. Block of bias currents
5. Clock splitter + DWA-correction of capacitors' mismatch

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC SiGe BiCMOS 180 nm
Status silicon proven
Area 0.144 mm^2

7.2 ELECTRICAL CHARACTERISITCS

The values of electrical parameters are given for V_{dd} = 1.65 ÷ 1.95 V and T_j = -45 ÷ +85 °C, unless otherwise specified; typical values are given for V_{dd} = 1.8 V and T_j = 27 °C.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{dd}	-	1.65	1.8	1.95	V
Reference voltage	V_{ref}	-	0.5	0.9	1.3	V
Operating temperature	T_j	-	-45	27	+85	°C
Clock frequency	F_{clk}	-	8	25	32	MHz
Sampling rate	F_S	-	-	800	-	kSPS
Duty cycle	S	-	45	50	55	%
Oversampling ratio	OSR	-	8	32	40	-
Signal bandwidth	BW	-	400	-	500	kHz
Signal to noise ratio	SNR	-	43.24	77.75	82.87	dB
Stand-by power	P_{std}	-	0.014	0.023	0.054	uW
Supply power	P_{supply}	-	2.13	3.19	3.78	mW
Common mode voltage	U	-	-	0.9	-	V
Supply current	I_{supply}	-	1.29	1.77	1.94	mA
Input high-logic level	V_{IH}	For digital inputs	$0.7V_{dd}$	-	V_{dd}+0.25	V
Input low-logic level	V_{IL}		-0.25	-	$0.3V_{dd}$	V

8 TYPICAL CHARACTERISTICS

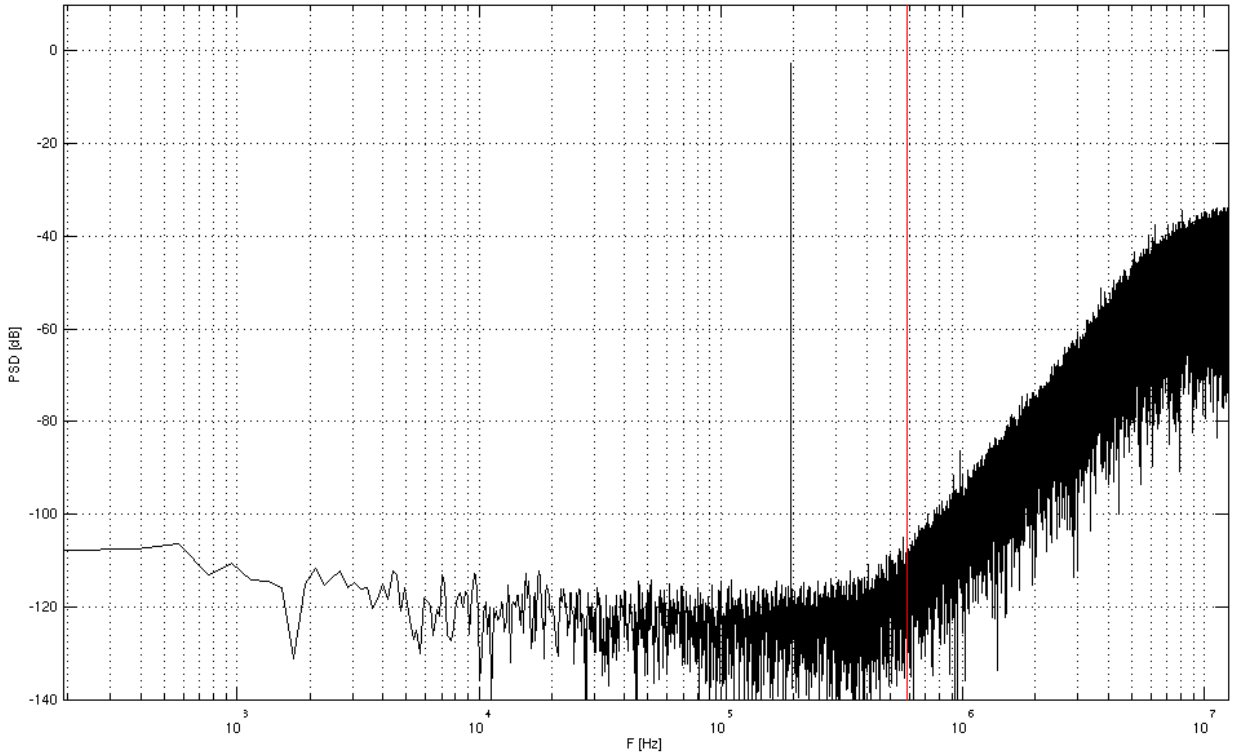

Figure 3: Output signal spectrum. Conditions:
Fin = 200 kHz, Fclk = 25 MHz, Vin (dif p-p) = 1280 mV, SNR (in band) = 81.71 dB

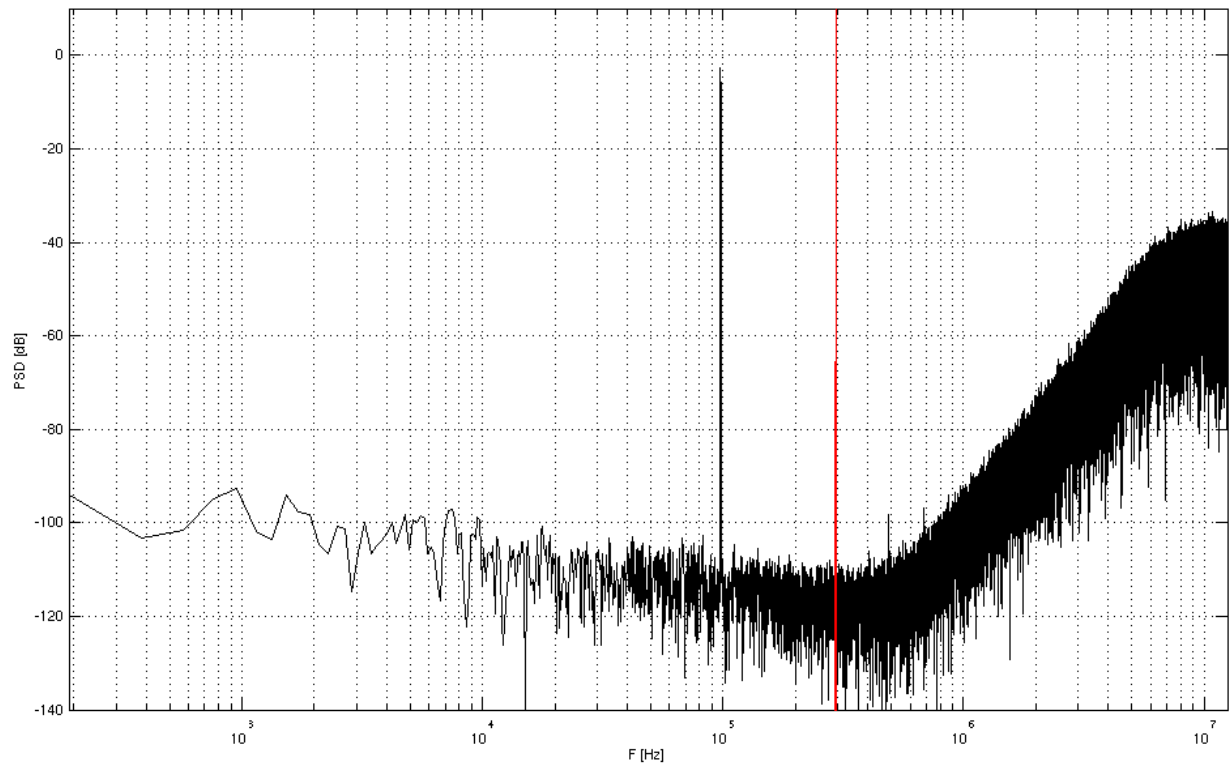

Figure 4: Output signal spectrum. Conditions:
Fin = 125 kHz, Fclk = 32 MHz, Vin (dif p-p) = 1280 mV, SNR (in band) = 77.75 dB

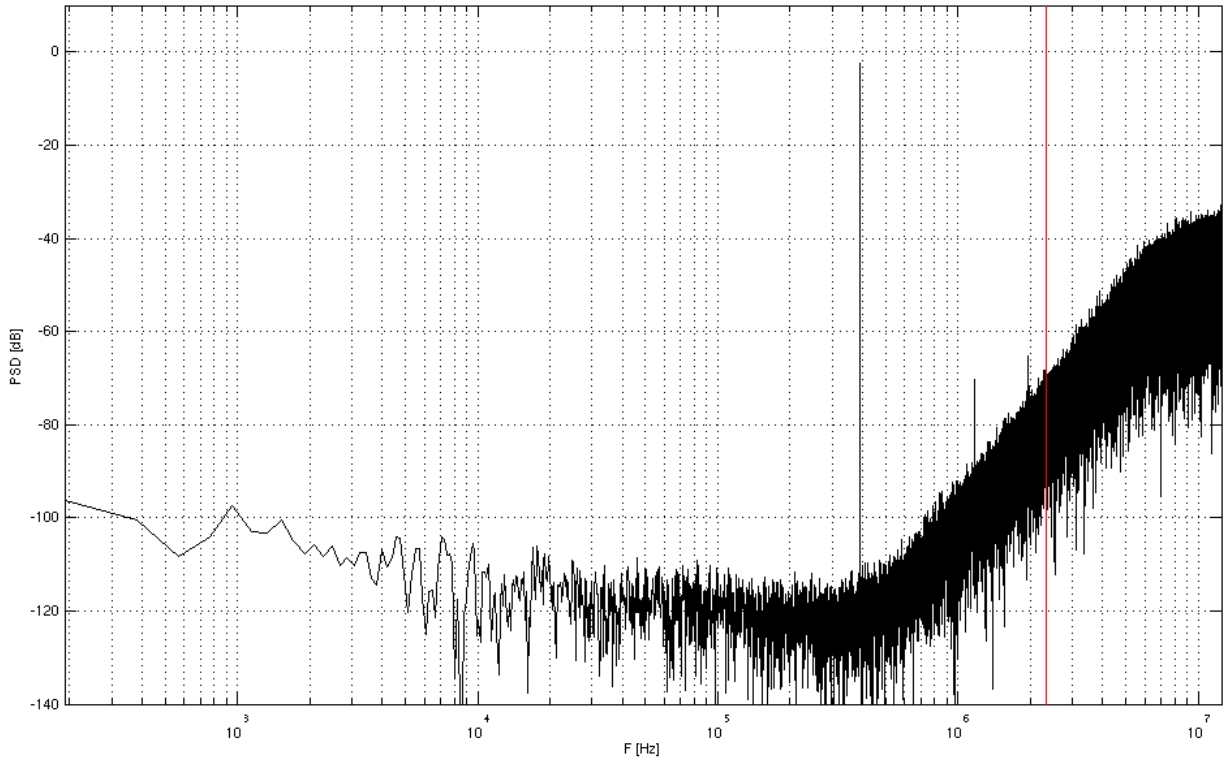

Figure 5: Output signal spectrum. Conditions:
Fin = 125 kHz, Fclk = 8 MHz, Vin (dif p-p) = 1280 mV, SNR (in band) = 43.27 dB

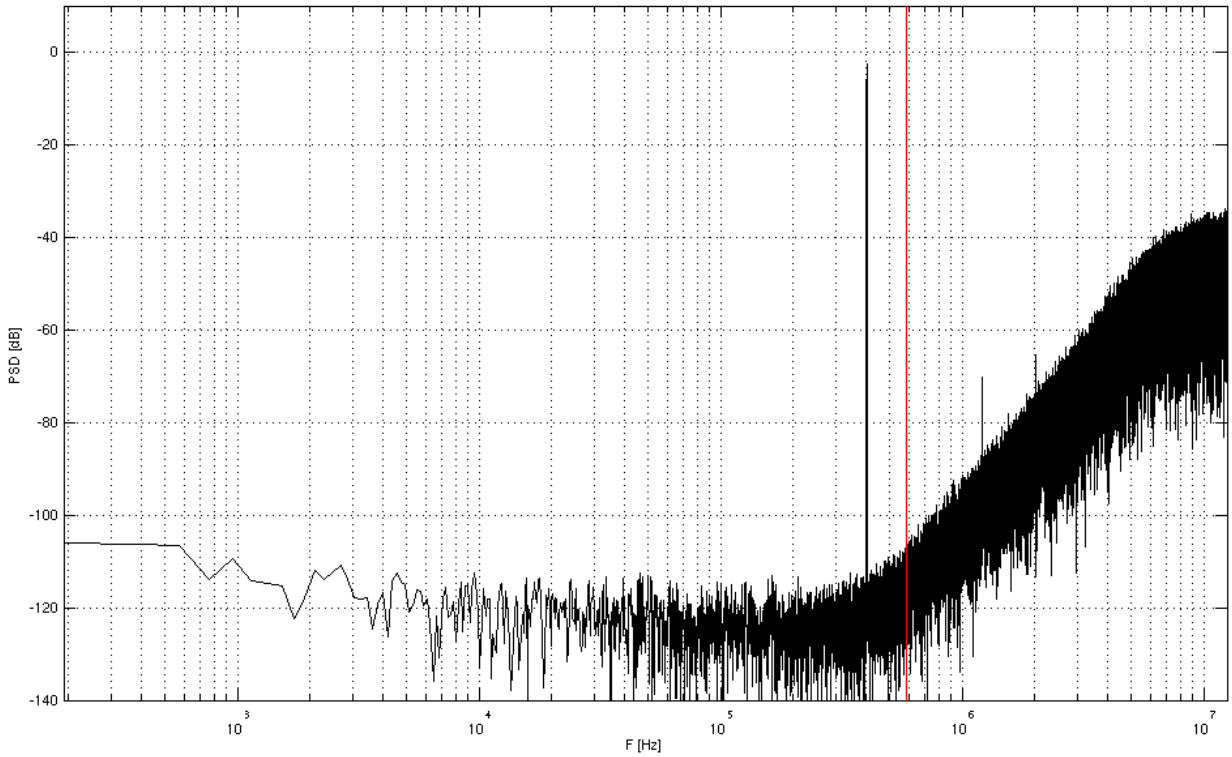

Figure 6: Output signal spectrum. Conditions:
Fin = 402 kHz, Fclk = 25 MHz, Vin (dif p-p) = 1280 mV, SNR (in band) = 82.87 dB

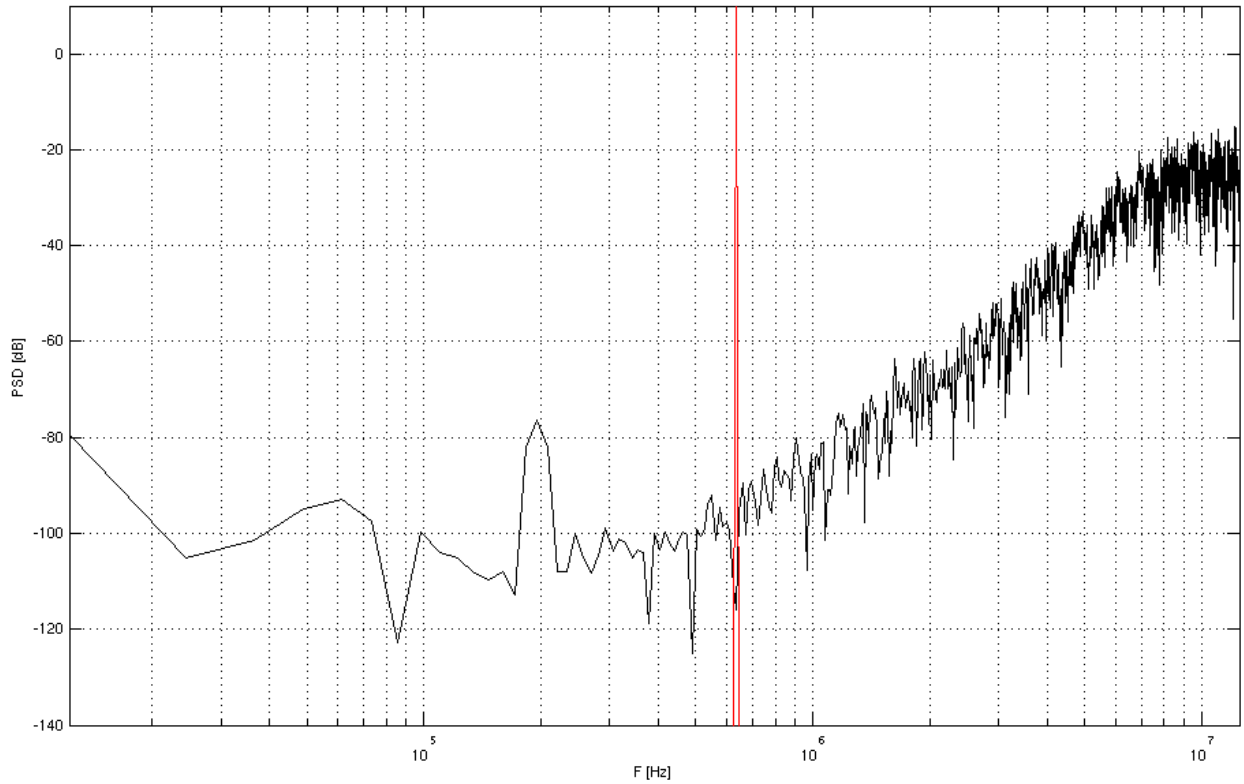

Figure 7: Output signal spectrum. Conditions:
Fin = 200 kHz, Fclk = 25 MHz, Vin (dif p-p) = 0.8 mV, SNR (in band) = 8.38 dB
Real reference voltages, input signal from IFA

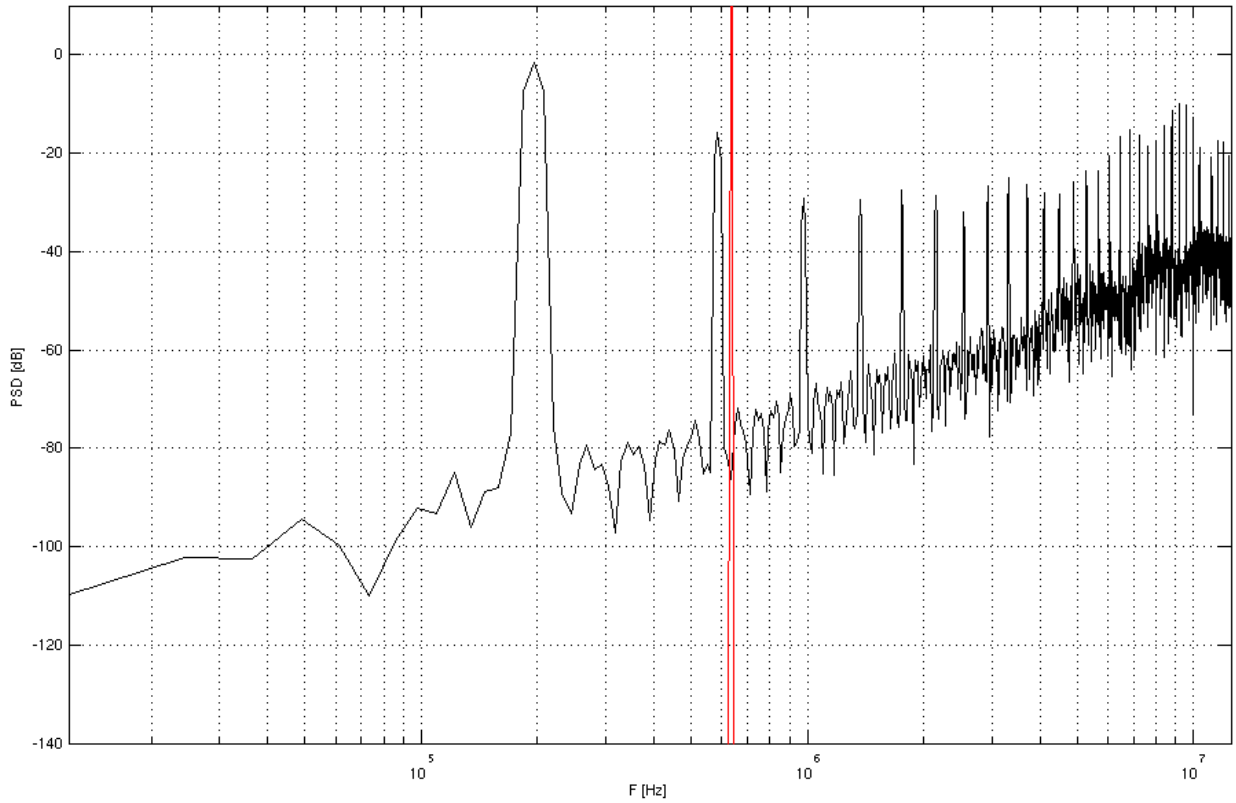

Figure 8: Output signal spectrum. Conditions:
Fin = 200 kHz, Fclk = 25 MHz, Vin (dif p-p) = 2560 mV (overload test), SNR = 14.29 dB

9 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation