44/70/90 MSPS 12-bit 1-channel ADC

SPECIFICATION

1 FEATURES

- TSMC 180 nm CMOS technology
- High speed pipelined ADC
- 1-channel
- Resolution 12 bit
- Conversion rate 44 – 90 MHz
- Different power supplies for digital (1.8 V) and analog (1.8 V) parts
- Low standby current 0.2 uA
- Low power dissipation:
  59.4 mW at 44 MSPS
  84.6 mW at 70 MSPS
- Total Harmonic Distortion (THD):
  -70.6 dB at 44 MSPS and F_{IN} = 1.9 MHz
  -70.1 dB at 70 MSPS and F_{IN} = 1.9 MHz
- Spurious-free dynamic range (SFDR):
  72.7 dB at 44 MSPS and F_{IN} = 1.9 MHz
  73 dB at 70 MSPS and F_{IN} = 1.9 MHz
- Signal-to-noise ratio (SNR):
  61.6 dB at 44 MSPS and F_{IN} = 1.9 MHz
  62.4 dB at 70 MSPS and F_{IN} = 1.9 MHz
- Compact die area 1.44 mm^2
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Optical networking
- Test equipment
- Portable ultrasound and digital beam-forming systems
- Telecommunication systems
- High quality imaging video systems
- WiFi, WiMax
- Mobile Communications
- High quality imaging video systems
- Data acquisition systems

3 OVERVIEW

The low-power high-speed 12-bit ADC employs high-performance differential pipeline architecture. The ADC consists of a core ADC, output logic, timing generation, reference currents circuits. The ADC requires: 1.7 ÷ 2 V analog supply, 1.7 ÷ 2 V digital supply, differential reference voltages 1.15 V and 0.65 V, common mode voltage 0.85 ÷ 1 V, reference current 9.9 ÷ 10.1 uA and differential input clock. The ADC supports standby mode which allows state with minimum power consumption. There is also the ability to configure the operating modes of the ADC by using digital registers.
The block is designed on TSMC 180 nm CMOS technology.

4 STRUCTURE

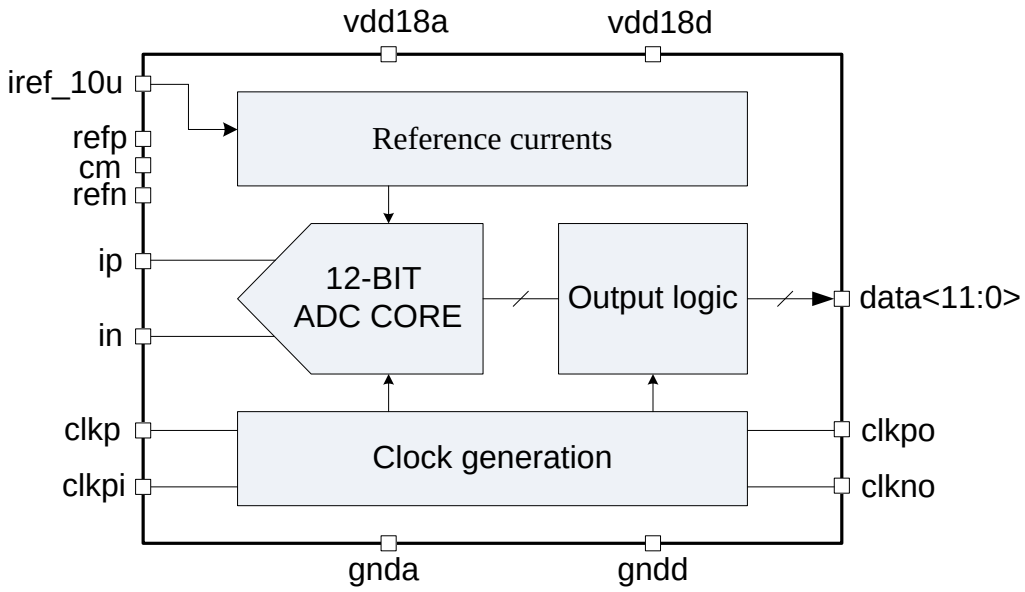

Figure 1: Functional block diagram structure

5 FUNTIONAL DESCRIPTION

The analog input voltage is sampled t_{d1} time after the positive edge of the conversion clock. Digital output data is latched after the pipeline conversion latency of 4 clock cycles.

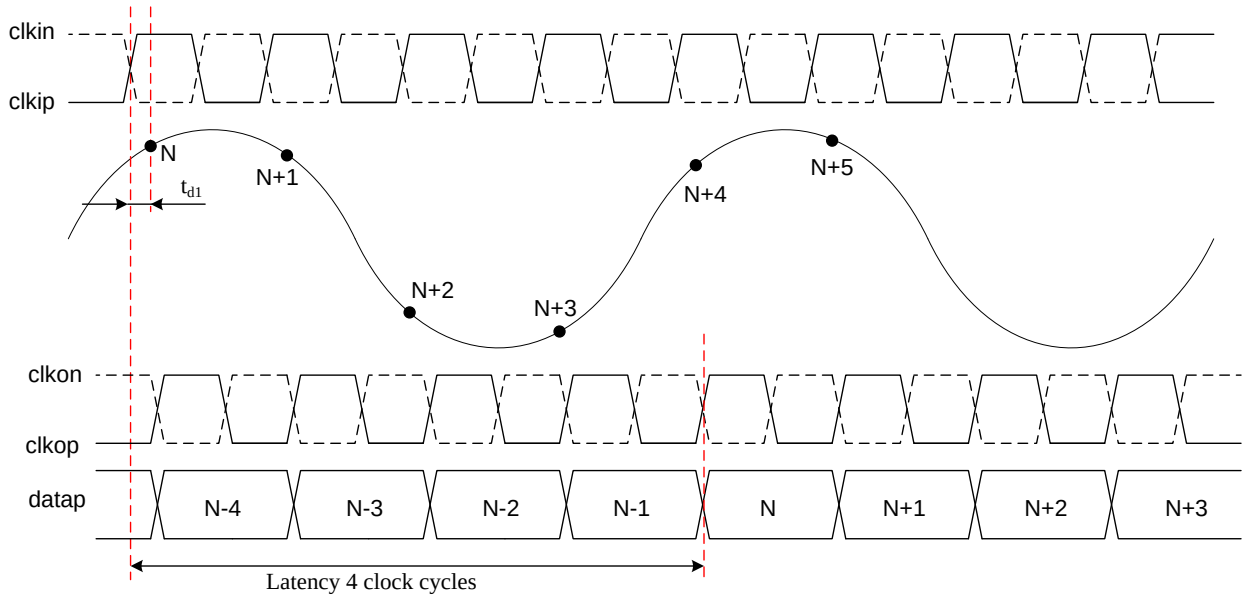

Figure 2: Timing diagram for normal operation

6 PIN DESCRIPTION

Name	Direction	Description
Analog Signals		
iref_10u	I	Reference current (10 uA)
ip	I	Differential analog inputs
in	I	
refp	I	Differential reference voltages
refn	I	
cm	I	Common mode voltage
Digital inputs		
clkp	I	Differential clock input
clkpi	I	
en	I	Enable
Digital outputs		
data<11:0>	O	Output data
clkpo	O	Differential output clock
clkno	O	
Test inputs		
adj_mdac_c1<4:0>	I	Bias control registers of MDACs
adj_mdac_c2<4:0>	I	
adj_mdac_c3<4:0>	I	
adj_sh<4:0>	I	Bias control registers of sample-and-hold circuit
adj_clk_comp<2:0>	I	Clock control register
adj_icomp<2:0>	I	Bias control registers of comparators
Supply Voltages		
vdd18a	I/O	Analog blocks supply voltage 1.8 V
vdd18d	I/O	Digital blocks supply voltage 1.8 V
gnda	I/O	Digital blocks ground
gndd	I/O	Analog blocks ground

7 LAYOUT DESRIPTION

7.1 TECHNOLOGY OPTIONS

ADC is designed under TSMC 180 nm CMOS technology process with following options:

- 4x1z metal option
- 1.8 V standard Vt MOS
- 1.5 fF/um^2 MIM capacitor
- P+ polysilicon OP resistor

7.2 PHYSICAL DIMENTIONS

ADC layout dimensions are given in the table 1.

Table 1: ADC dimensions

Dimension	Value	Unit
Height	600	um
Width	2400	um

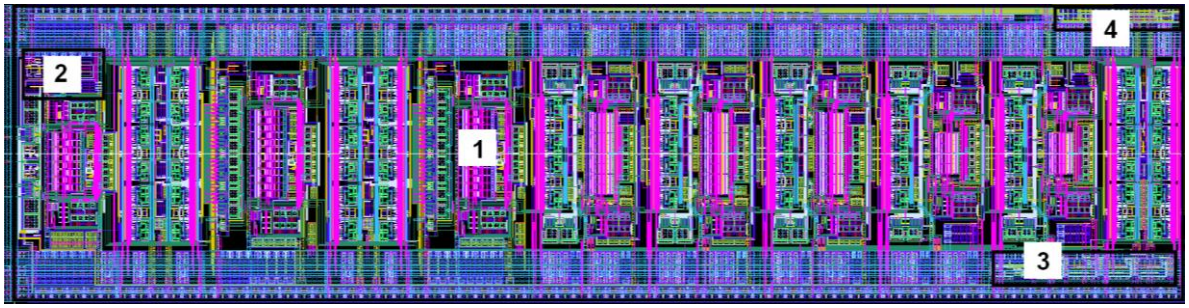

Figure 3: ADC layout view

1. Core ADC
2. Reference currents
3. Timing generation
4. Output logic

8 INTEGRATION GUIDELINES

8.1 PLACE AND ROUTE GUIDELINES

1) ADC analog inputs ip and in signals should be connected to analog IO PADs or an internal analog circuits (intermediate frequency amplifier, filter). IO PADs should not have an internal resistor to increase bandwidth.
2) Wiring of analog inputs should be symmetrical and as short as possible.
3) Noisy, power and high-frequency circuits should not place near ADC.
4) Minimum space 40 um between ADC and other circuits should be kept.
5) Minimum ultra thick metal wiring width is 25 um for vdd18a and gnda. Multiple layers of metal can be used to reduce layout space.
6) Minimum ultra thick metal wiring width is 25 um for vdd18d and gndd. Multiple layers of metal can be used to reduce layout space.
7) Allowable total resistance of vdd18a and gnda are 0.1 Ohm. Blocking capacitors should be added and placed as close as possible.
8) Allowable total resistance of vdd18d and gndd are 0.2 Ohm. Blocking capacitors should be added and placed as close as possible.
9) The ADC requires off-chip capacitors on pins refp, cm and refn. The refp, cm and refn pins should be bypassed as shown in figure 4. The 100 nF capacitors between refp and refn should be as close to pins as possible.

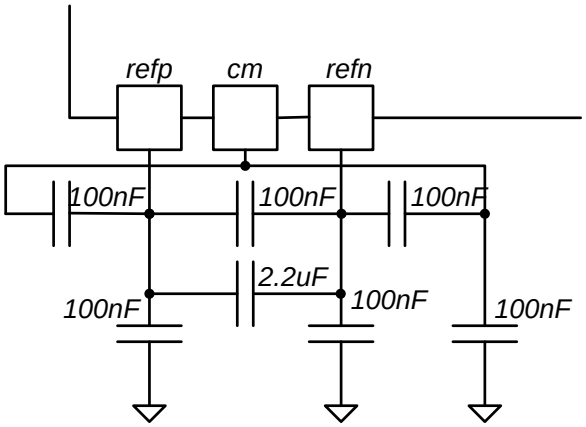

Figure 4: Capacitors on pins refp, cm and refn

9 OPERATING CHARACTERISTICS

9.1 TECHNICAL CHARACTERISTICS

Technology TSMC 180nm CMOS
Status silicon proven
Area 1.44 mm^2

9.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{DDA} = V_{DDD} = 1.7$ V ÷ 2 V, $T_j = 27$ C, $A_{IN} = –1$ dBFS, unless otherwise noted. Typical values are at $V_{DDA} = V_{DDD} = 1.8$ V, $T_j = 27$ C

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
Junction temperature	T_j	-	-40	27	+85	°C
Analog blocks supply voltage	V_{DDA}	-	1.7	1.8	2	V
Digital blocks supply voltage	V_{DDD}	-	1.7	1.8	2	V
Reference current	I_{REF}	-	9.9	10	10.1	uA
Resolution	N	-	-	12	-	bit
Sample rate	F_S	-	-	44	90	MHz
Standby current	I_{ST}	$V_{DDA} + V_{DDD}$	-	0.2	-	uA
Full power bandwidth	B	-	-	45	-	MHz
Current consumption	I_{CN}	$V_{DDA} + V_{DDD}$, $F_S = 44$ MHz	-	33	-	mA
		$V_{DDA} + V_{DDD}$, $F_S = 70$ MHz	-	47	-	
		$V_{DDA} + V_{DDD}$, $F_S = 90$ MHz	-	59	-	
Total power consumption	P_{TOTAL}	$V_{DDA} + V_{DDD}$, $F_S = 44$ MHz	-	59.4	-	mW
		$V_{DDA} + V_{DDD}$, $F_S = 70$ MHz	-	84.6	-	
		$V_{DDA} + V_{DDD}$, $F_S = 90$ MHz	-	106.2	-	
Differential input voltage range	$A_{IN\ p\text{-}p}$	-	-	1	-	V p-p
Differential reference voltages	V_{REFP}	-	-	V_{CM} +0.25	-	V
	V_{REFN}	-	-	V_{CM} - 0.25	-	V
Input common mode voltage	V_{CM}	-	-	0.5 V_{DDA}	-	V
Clock input duty cycle	S	-	45	50	55	%
Input logic high level	V_{IH}	For digital inputs	0.7 V_{DDD}	-	-	V
Input logic low level	V_{IL}		-	-	0.3 V_{DDD}	V

9.3 DYNAMIC CHARACTERISTICS

The values of electrical characteristics are specified for $V_{DDA} = V_{DDD} = 1.7$ V ÷ 2 V, $T_a = 27$ C , $A_{IN} = –1$ dBFS, unless otherwise noted. Typical values are at $V_{DDA} = V_{DDD} = 1.8$ V, $T_a = 27$ C

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
F_S = 44 MHz						
Spurious free dynamic range	SFDR	F_{IN} = 1.9 MHz	70.9	72.7	73.3	dB
		F_{IN} = 2.5 MHz	68.5	72.3	73.1	
		F_{IN} = 5 MHz	69.2	72.1	73	
		F_{IN} = 10.7 MHz	70	71.4	72.7	
Total harmonic distortion	THD	F_{IN} = 1.9 MHz	-75.3	-70.6	-67.8	dB
		F_{IN} = 2.5 MHz	-75	-70.4	-67.5	
		F_{IN} = 5 MHz	-75	-71.1	-68	
		F_{IN} = 10.7 MHz	-74.6	-69.6	-67.5	
Signal-to-noise ratio	SNR	F_{IN} = 1.9 MHz	61.5	61.6	62.2	dB
		F_{IN} = 2.5 MHz	61.4	61.5	62.4	
		F_{IN} = 5 MHz	61.4	61.5	62.9	
		F_{IN} = 10.7 MHz	60.8	61.4	61.6	
Signal-to-noise and distortion ratio	SINAD (SNDR)	F_{IN} = 1.9 MHz	61	61.1	61.5	dB
		F_{IN} = 2.5 MHz	60.5	60.9	61.3	
		F_{IN} = 5 MHz	60.8	61.1	61.8	
		F_{IN} = 10.7 MHz	60.2	60.9	61.1	
Effective number of bits	ENOB	F_{IN} = 1.9 MHz	9.84	9.86	9.92	bits
		F_{IN} = 2.5 MHz	9.76	9.82	9.89	
		F_{IN} = 5 MHz	9.81	9.86	9.97	
		F_{IN} = 10.7 MHz	9.71	9.82	9.86	
Two-tone intermodulation distortion	IMD	F_{IN1} = 2 MHz, F_{IN2} = 2.5 MHz, $A_{IN1} = A_{IN2}$ = -7 dBFS	-	70.5	-	dB
		F_{IN1} = 4 MHz, F_{IN2} = 5 MHz, $A_{IN1} = A_{IN2}$ = -7 dBFS	-	71	-	
		F_{IN1} = 10.2 MHz, F_{IN2} = 11.2 MHz, $A_{IN1} = A_{IN2}$ = -7 dBFS	-	73.6	-	
Differential nonlinearity	DNL	F_{IN} = 1.9 MHz	-	0,89	-	LSB
Integral nonlinearity	INL	F_{IN} = 1.9 MHz	-	2,84	-	LSB

Table “Dynamic characteristics” (continue)

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
F_S = 70 MHz						
Spurious free dynamic range	SFDR	F_{IN} = 1.9 MHz	70.5	73	75	dB
		F_{IN} = 2.5 MHz	69	70	73.6	
		F_{IN} = 5 MHz	67	67.5	70	
		F_{IN} = 10.7 MHz	61	63.1	65	
Total harmonic distortion	THD	F_{IN} = 1.9 MHz	-71.83	-70.1	-69.6	dB
		F_{IN} = 2.5 MHz	-73.3	-68	-67.8	
		F_{IN} = 5 MHz	-73.1	-70.3	-70.1	
		F_{IN} = 10.7 MHz	-70.27	-71.8	-67.67	
Signal-to-noise ratio	SNR	F_{IN} = 1.9 MHz	61.7	62.4	62.7	dB
		F_{IN} = 2.5 MHz	61.2	61.3	61.5	
		F_{IN} = 5 MHz	59.3	59.4	59.7	
		F_{IN} = 10.7 MHz	55.3	56.5	56.8	
Signal-to-noise and distortion ratio	SINAD (SNDR)	F_{IN} = 1.9 MHz	61.3	61.8	61.9	dB
		F_{IN} = 2.5 MHz	60.2	60.4	61.6	
		F_{IN} = 5 MHz	59	59.1	59.5	
		F_{IN} = 10.7 MHz	55.2	56.4	56.9	
Effective number of bits	ENOB	F_{IN} = 1.9 MHz	9.89	9.97	9.99	bits
		F_{IN} = 2.5 MHz	9.71	9.74	9.94	
		F_{IN} = 5 MHz	9.51	9.52	9.6	
		F_{IN} = 10.7 MHz	8.88	9.08	9.16	
Differential nonlinearity	DNL	F_{IN} = 1.9 MHz	-	1.09	-	LSB
Integral nonlinearity	INL	F_{IN} = 1.9 MHz	-	2.17	-	LSB

Table “Dynamic characteristics” (continue)

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
F_S = 90 MHz						
Spurious free dynamic range	SFDR	F_{IN} = 1.9 MHz	-	74.6	-	dB
		F_{IN} = 2.5 MHz	-	70.8	-	
		F_{IN} = 5 MHz	-	71.1	-	
		F_{IN} = 10.7 MHz	-	69.5	-	
Total harmonic distortion	THD	F_{IN} = 1.9 MHz	-	-72.4	-	dB
		F_{IN} = 2.5 MHz	-	-69.8	-	
		F_{IN} = 5 MHz	-	-68.4	-	
		F_{IN} = 10.7 MHz	-	69.3	-	
Signal-to-noise ratio	SNR	F_{IN} = 1.9 MHz	-	61.6	-	dB
		F_{IN} = 2.5 MHz	-	61.8	-	
		F_{IN} = 5 MHz	-	61.6	-	
		F_{IN} = 10.7 MHz	-	58.9	-	
Signal-to-noise and distortion ratio	SINAD (SNDR)	F_{IN} = 1.9 MHz	-	61.3	-	dB
		F_{IN} = 2.5 MHz	-	61.2	-	
		F_{IN} = 5 MHz	-	60.8	-	
		F_{IN} = 10.7 MHz	-	58.6	-	
Effective number of bits	ENOB	F_{IN} = 1.9 MHz	-	9.89	-	bits
		F_{IN} = 2.5 MHz	-	9.87	-	
		F_{IN} = 5 MHz	-	9.81	-	
		F_{IN} = 10.7 MHz	-	9.11	-	

10 TYPICAL CHARACTERISTICS

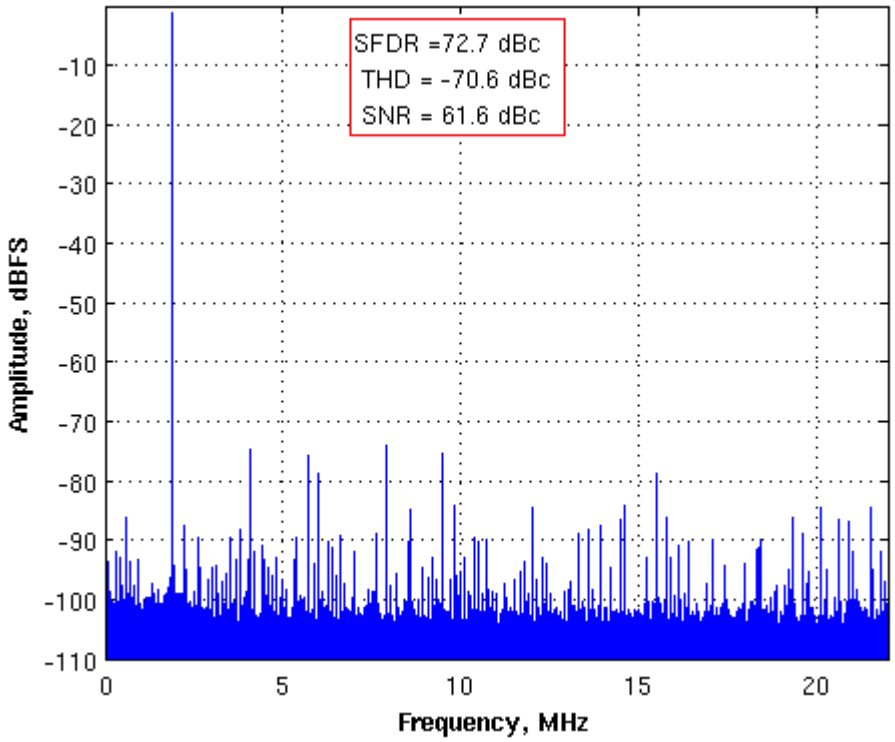

Figure 5: Single-tone FFT with F_{IN} = 1.9 MHz, F_S = 44 MHz, A_{IN} = –1 dBFS

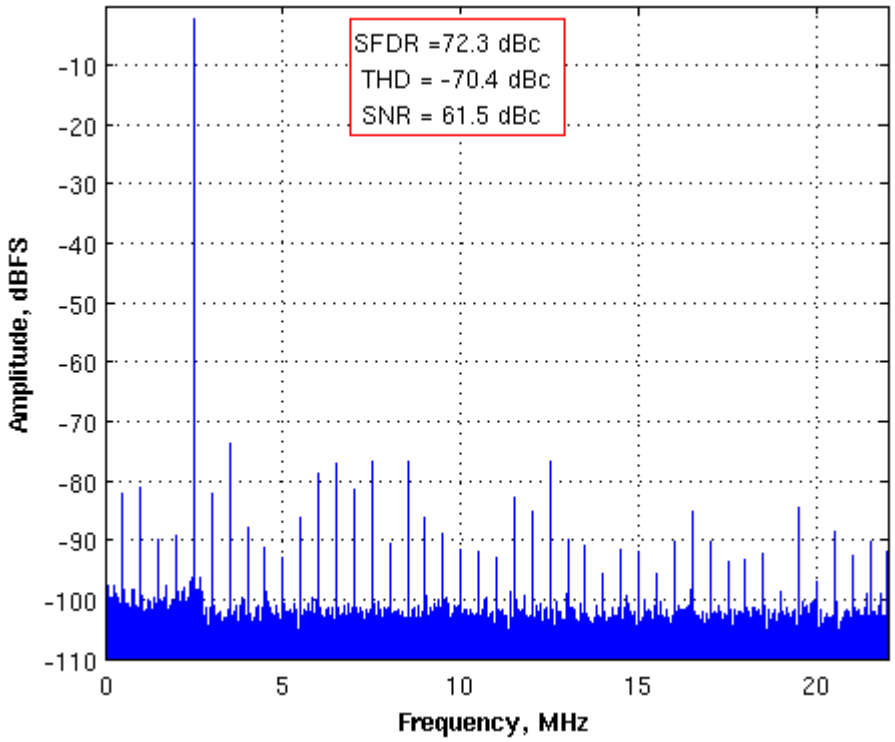

Figure 6: Single-tone FFT with F_{IN} = 2.5 MHz, F_S = 44 MHz, A_{IN} = –1 dBFS

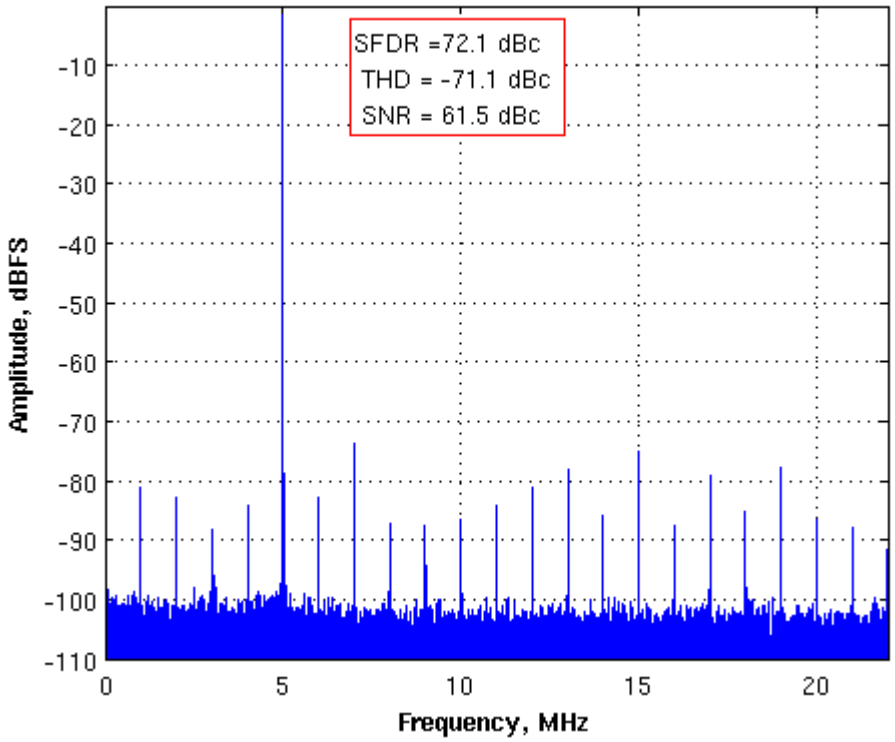

Figure 7: Single-tone FFT with F_{IN} = 5 MHz,
F_S = 44 MHz, A_{IN} = –1 dBFS

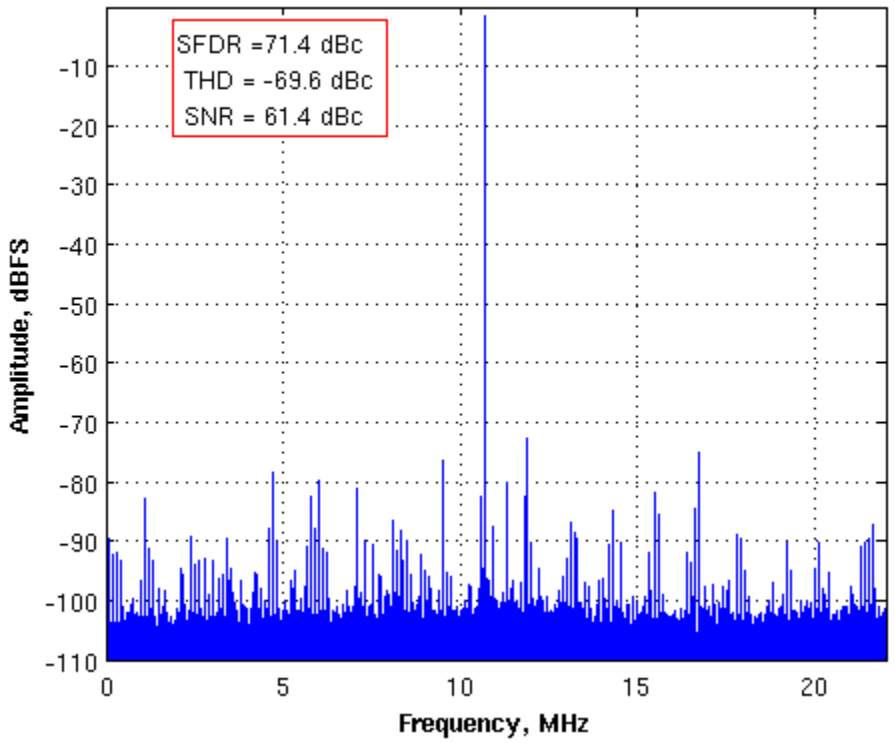

Figure 8: Single-tone FFT with F_{IN} = 10.7 MHz,
F_S = 44 MHz, A_{IN} = –1 dBFS

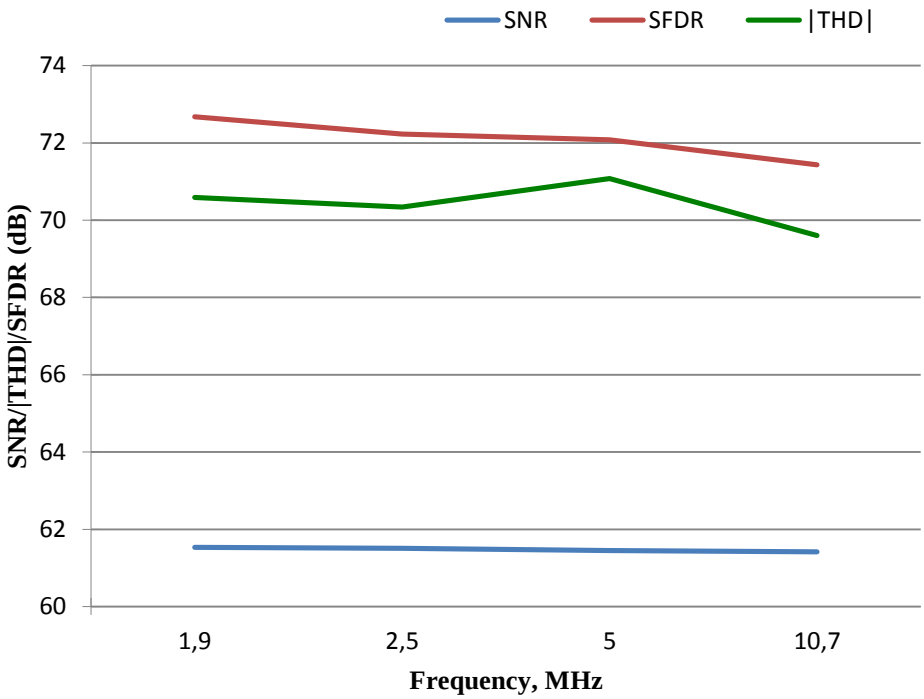

Figure 9: SNR/THD/SFDR vs. F_{IN}, F_S = 44 MHz

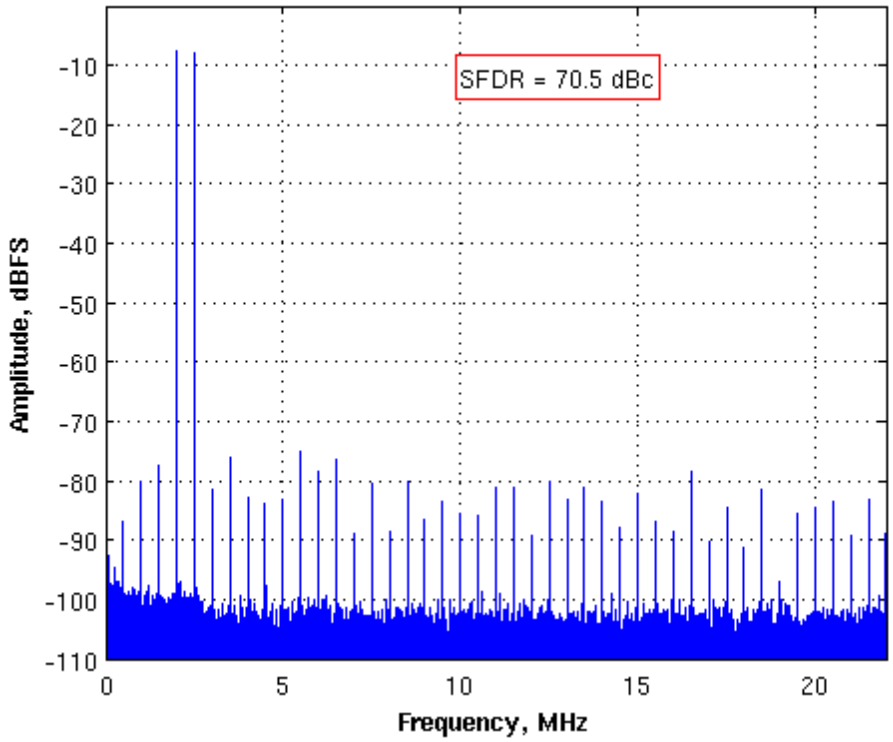

Figure 10: Two-tone FFT with F_{IN1} = 2 MHz, F_{IN2} = 2.5 MHz, F_S = 44 MHz, A_{IN1} = A_{IN2} = –7 dBFS

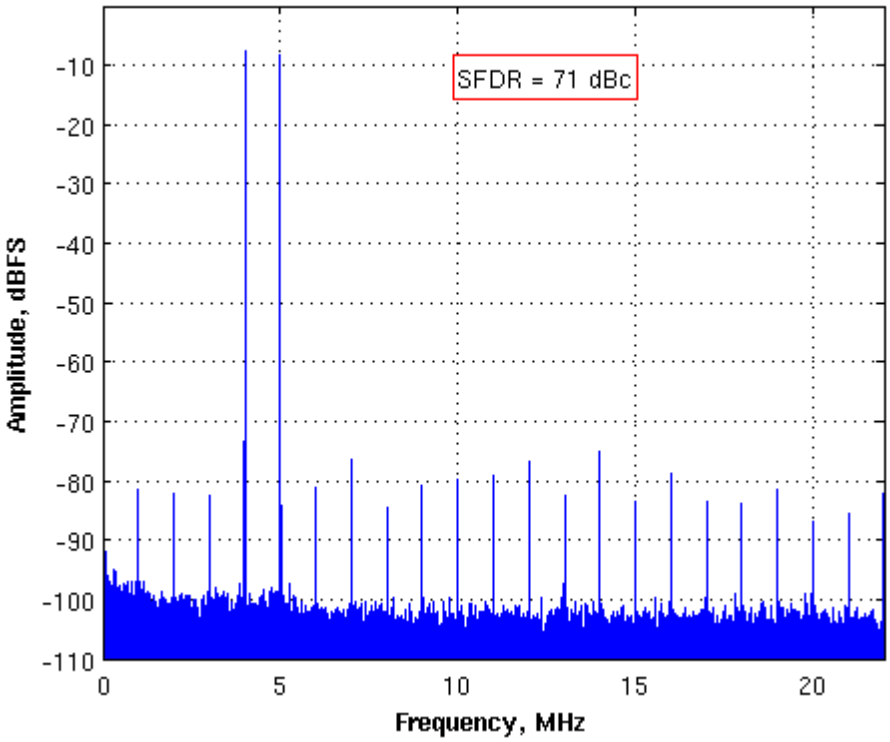

Figure 11: Two-tone FFT with F_{IN1} = 4 MHz, F_{IN2} = 5 MHz, F_S = 44 MHz, A_{IN1} = A_{IN2} = –7 dBFS

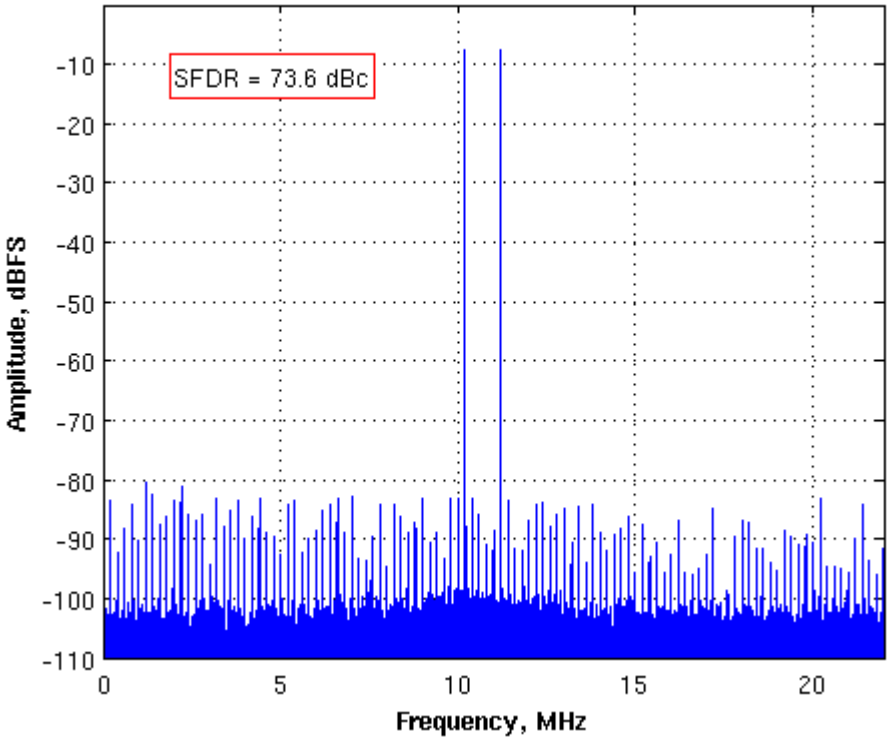

Figure 12: Two-tone FFT with F_{IN1} = 10.2 MHz, F_{IN2} = 11.2 MHz, F_S = 44 MHz, A_{IN1} = A_{IN2} = –7 dBFS

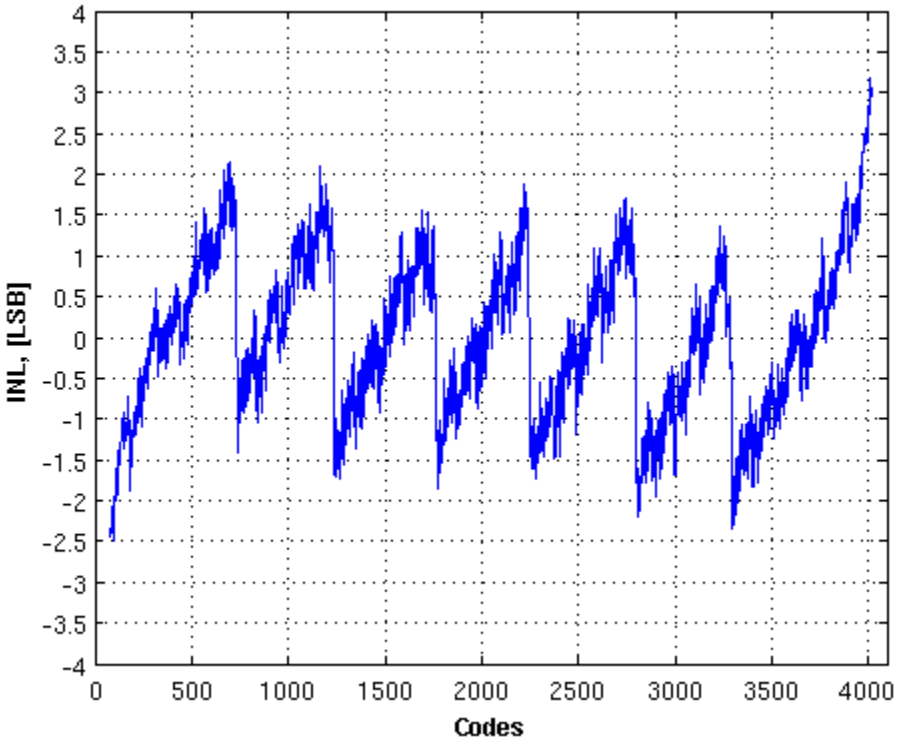

Figure 13: Integral nonlinearity (INL),
F_{IN} = 1.9 MHz, F_S = 44 MHz

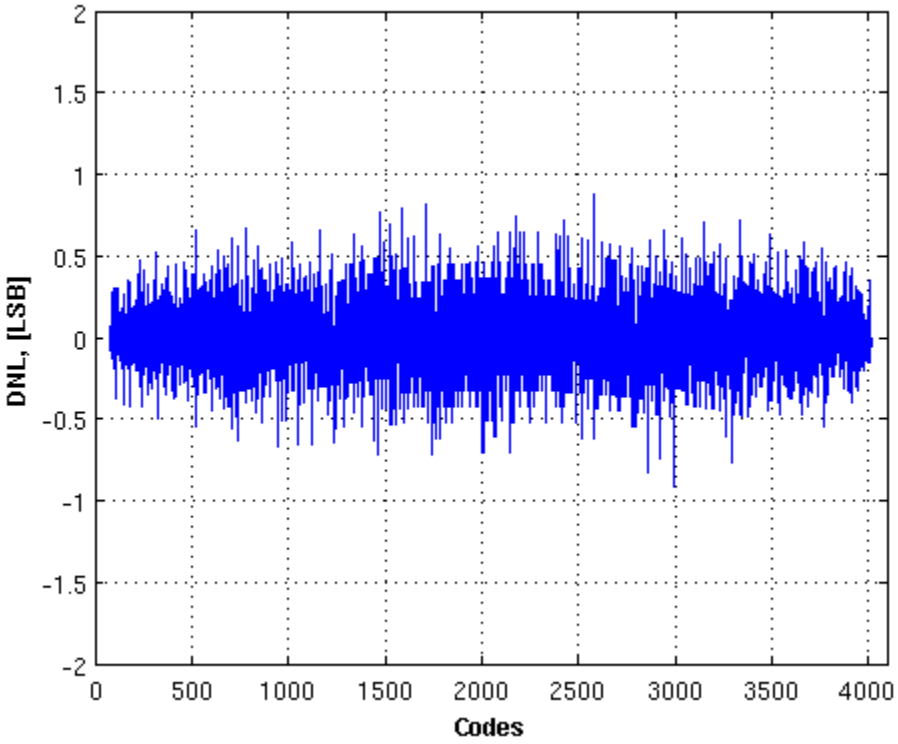

Figure 14: Differential nonlinearity (DNL),
F_{IN} = 1.9 MHz, F_S = 44 MHz

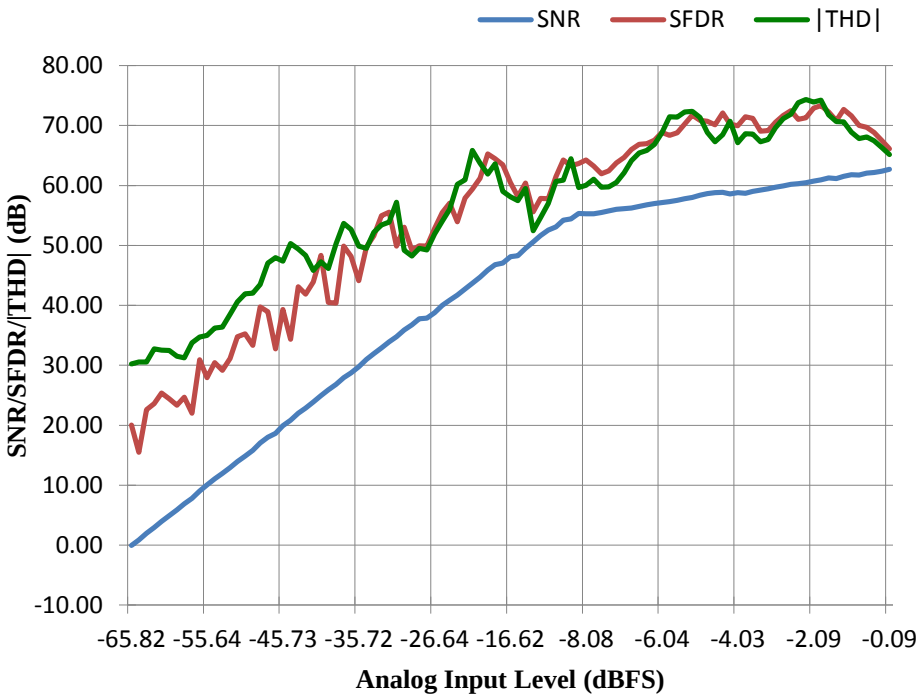

Figure 15: SNR/THD/SFDR vs. analog input level,
F_{IN} = 1.9 MHz, F_S = 44 MHz

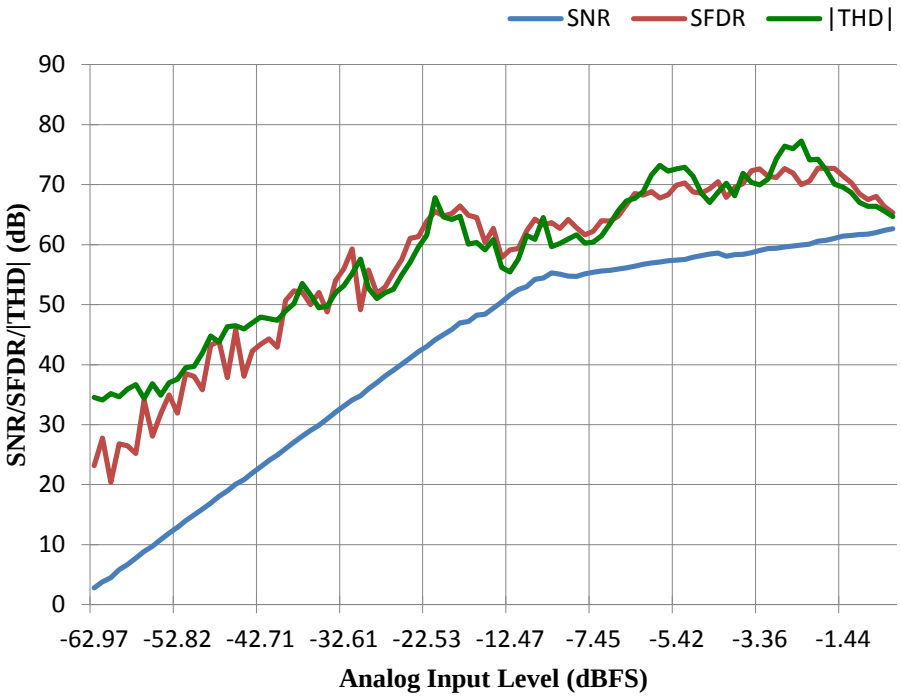

Figure 16: SNR/THD/SFDR vs. analog input level,
F_{IN} = 10.7 MHz, F_S = 44 MHz

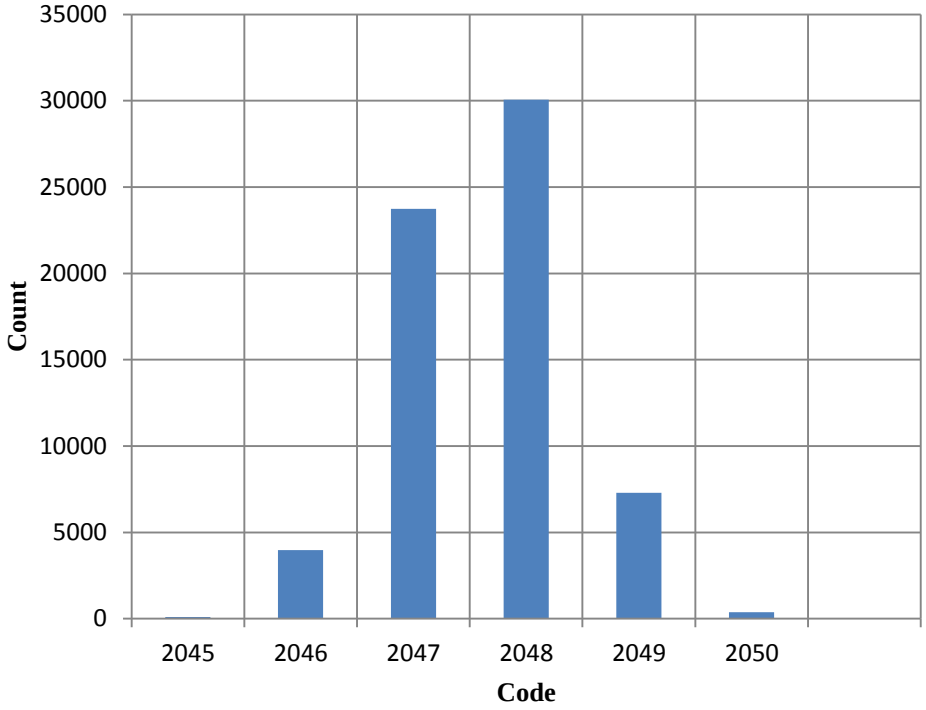

Figure 17: Grounded input histogram, F_S = 44 MHz

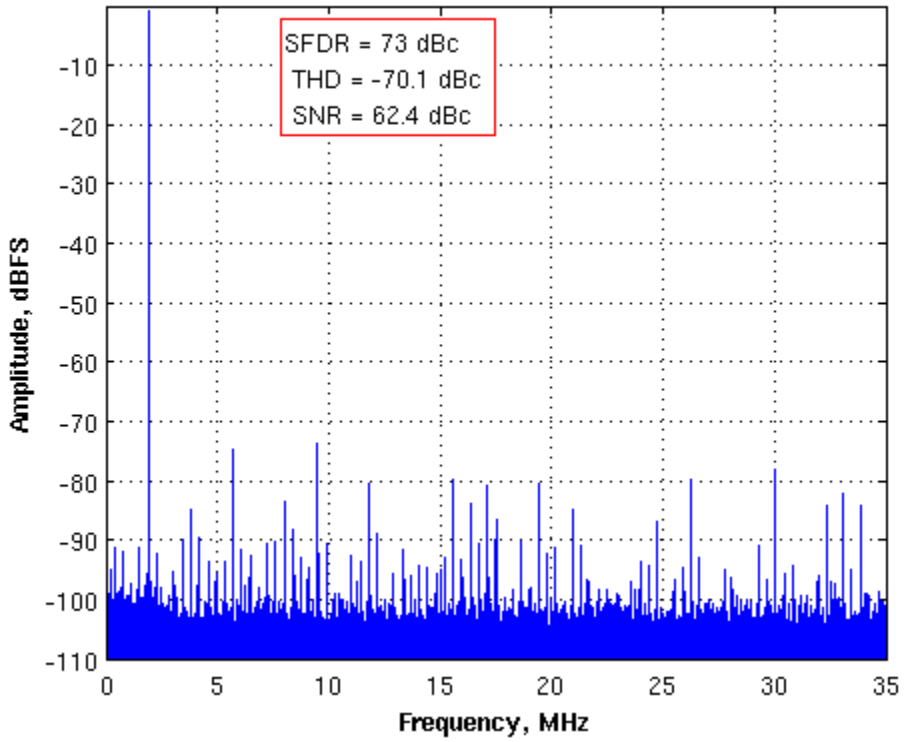

Figure 18: Single-tone FFT with F_{IN} = 1.9 MHz,
F_S = 70 MHz, A_{IN} = –1 dBFS

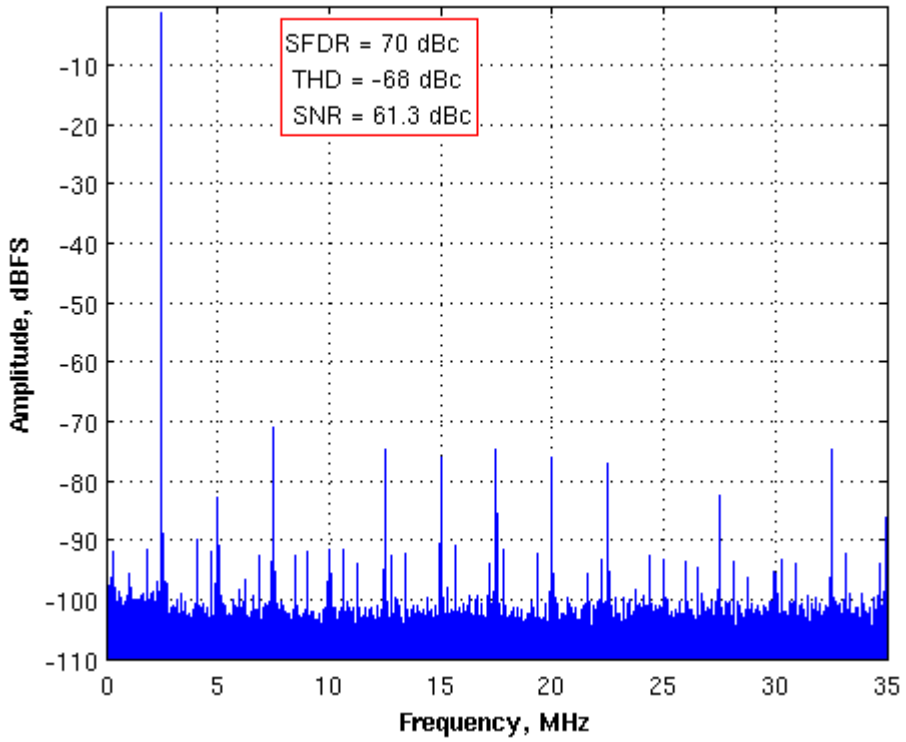

Figure 19: Single-tone FFT with F_{IN} = 2.5 MHz,
F_S = 70 MHz, A_{IN} = –1 dBFS

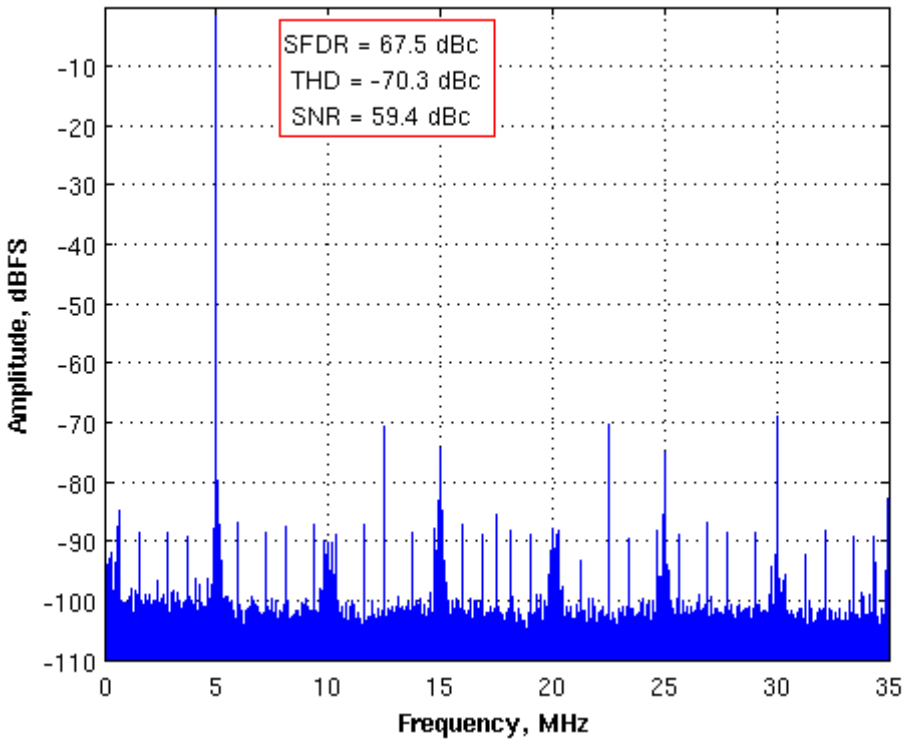

Figure 20: Single-tone FFT with F_{IN} = 5 MHz,
F_S = 70 MHz, A_{IN} = –1 dBFS

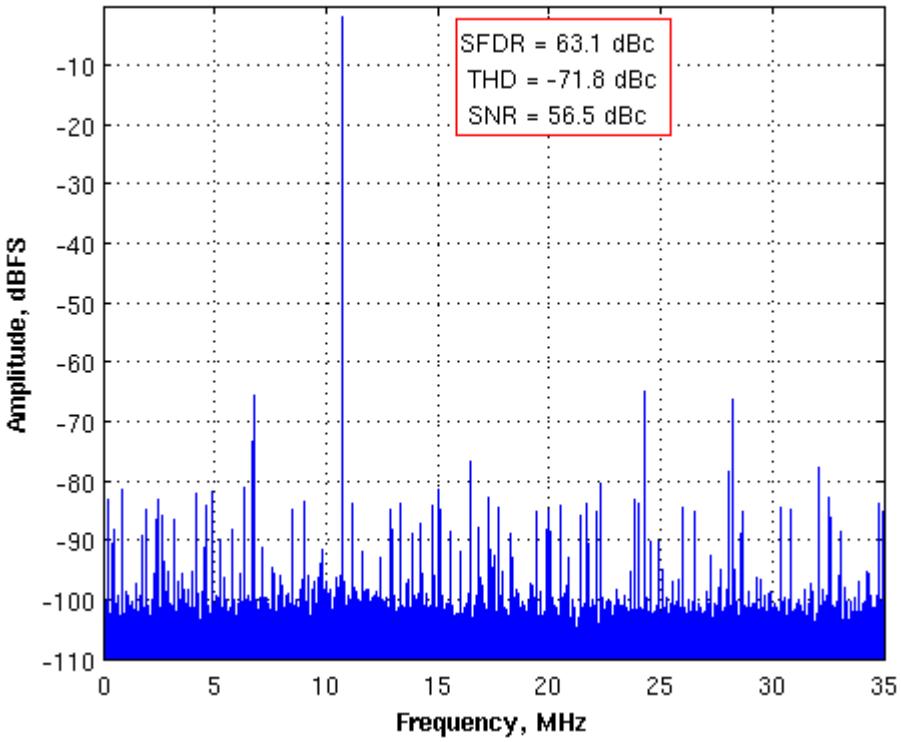

Figure 21: Single-tone FFT with F_{IN} = 10.7 MHz, F_S = 70 MHz, A_{IN} = –1 dBFS

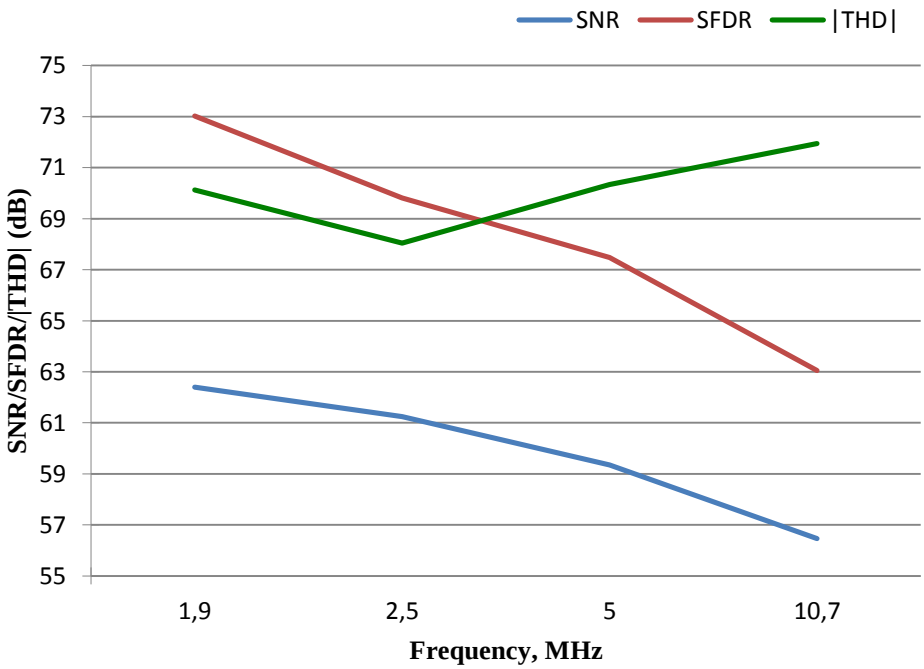

Figure 22: SNR/THD/SFDR vs. F_{IN}, F_S = 70 MHz

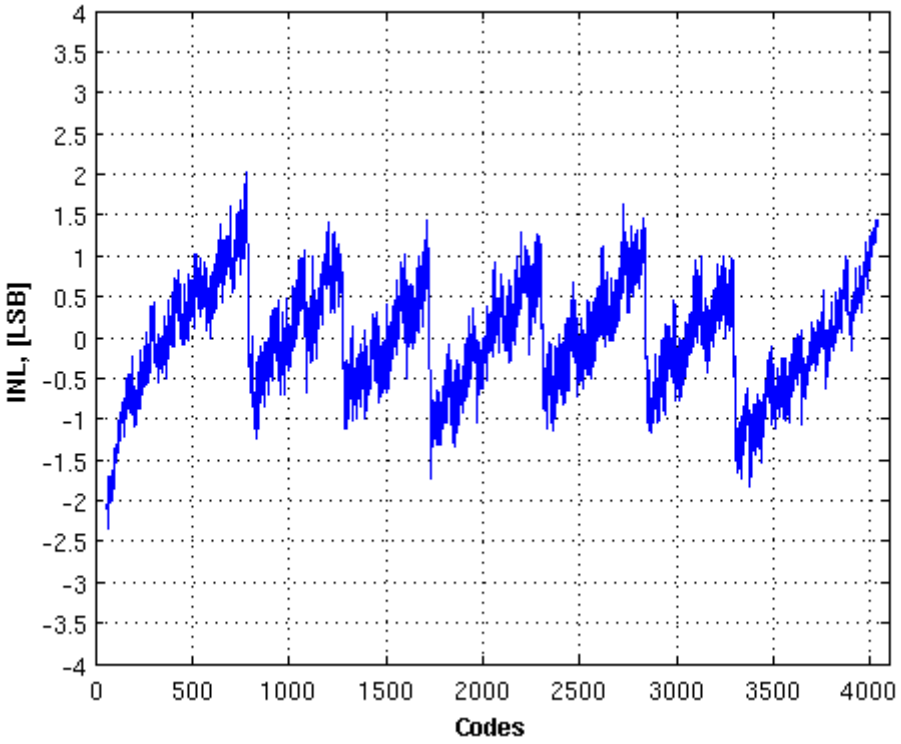

Figure 23: Integral nonlinearity (INL),
F_{IN} = 1.9 MHz, F_S = 70 MHz

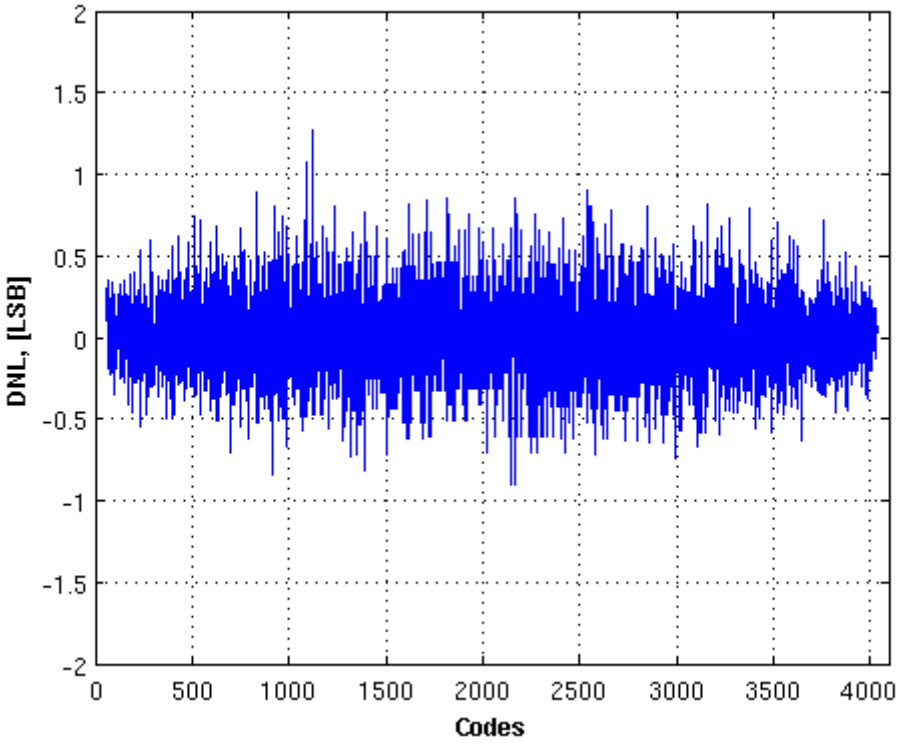

Figure 24: Differential nonlinearity (DNL),
F_{IN} = 1.9 MHz, F_S = 70 MHz

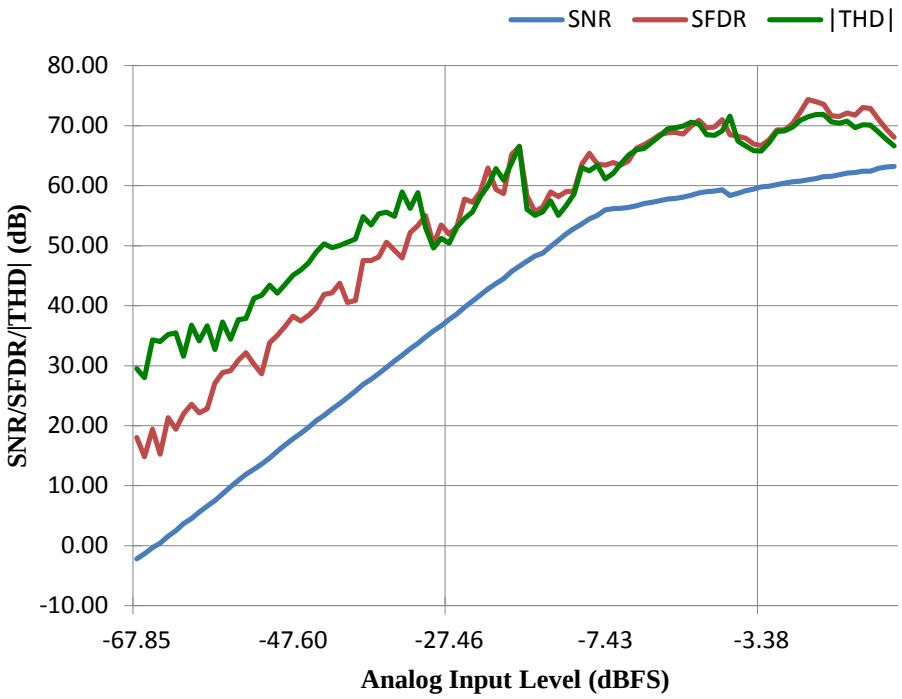

Figure 25: SNR/THD/SFDR vs. analog input level,
F_{IN} = 1.9 MHz, F_S = 70 MHz

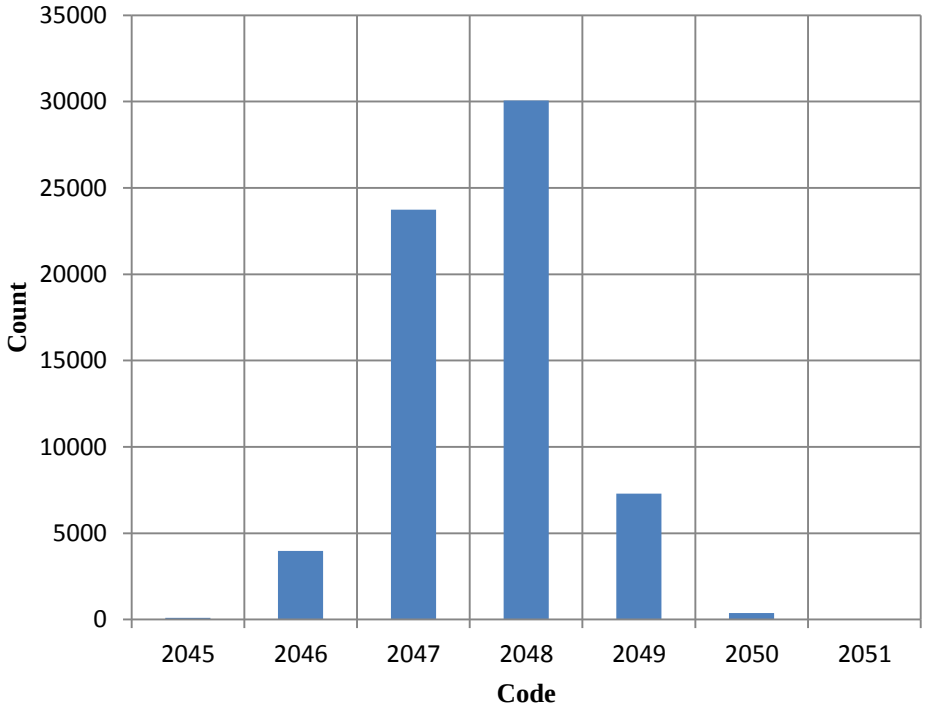

Figure 26: Grounded input histogram, F_S = 70 MHz

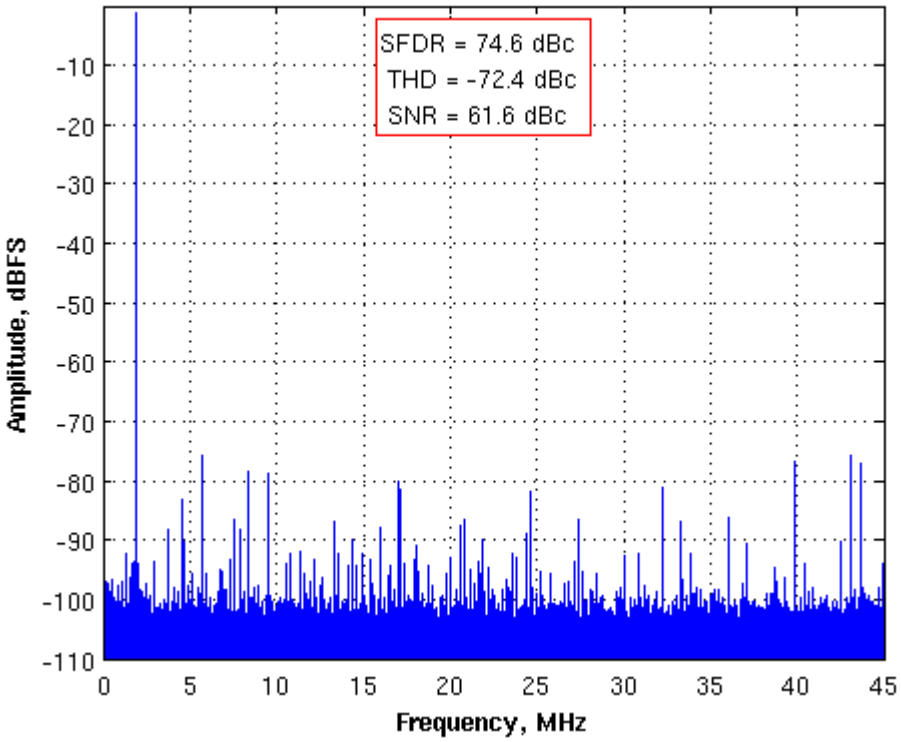

Figure 27: Single-tone FFT with F_{IN} = 1.9 MHz, F_S = 90 MHz, A_{IN} = –1 dBFS

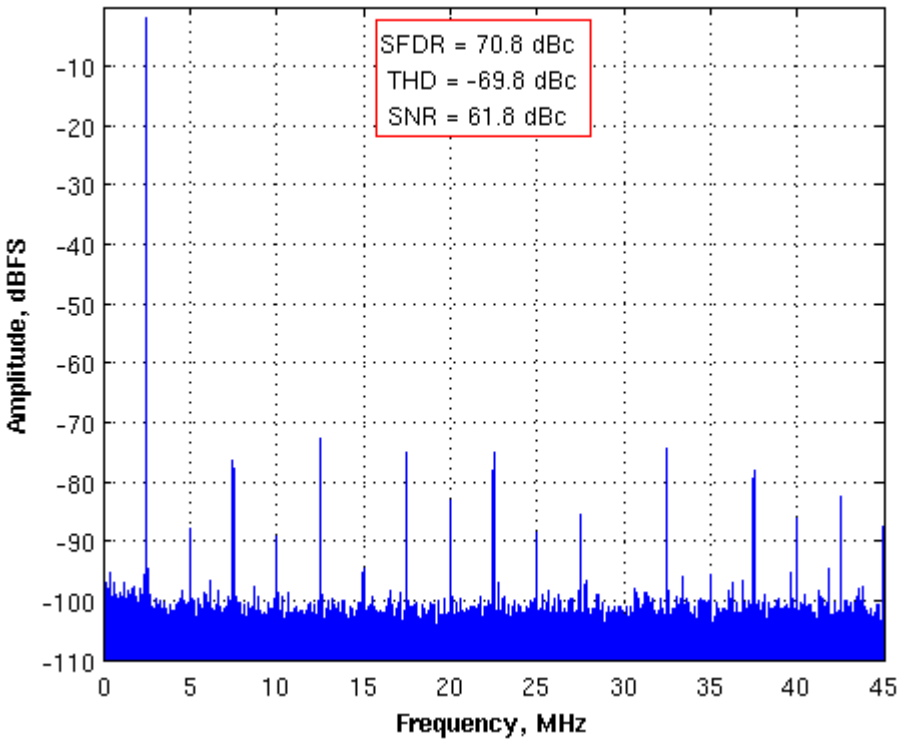

Figure 28: Single-tone FFT with F_{IN} = 2.5 MHz, F_S = 90 MHz, A_{IN} = –1 dBFS

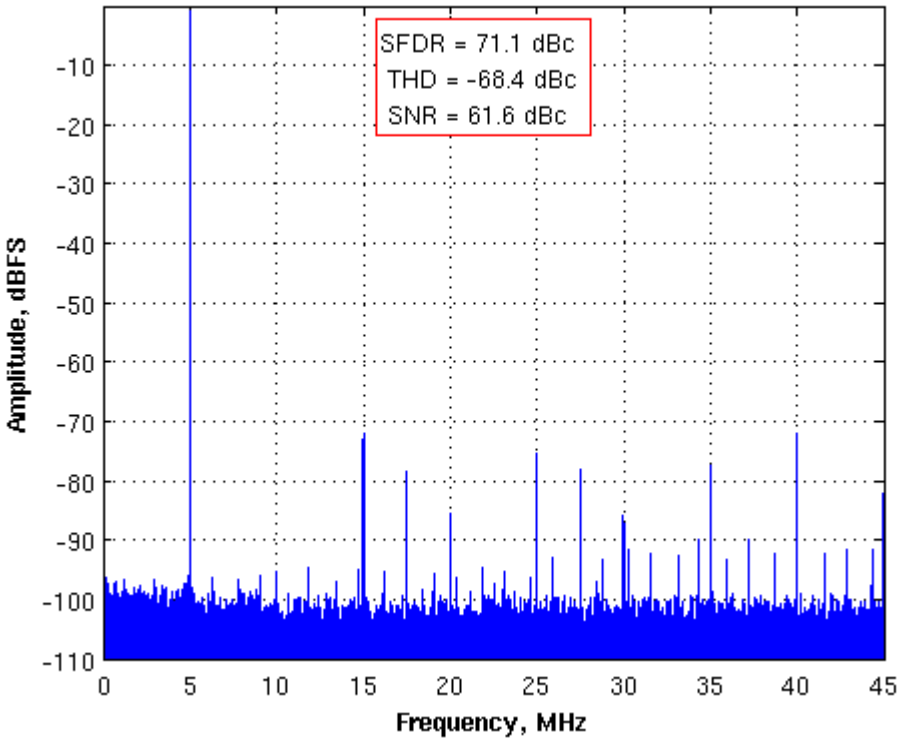

Figure 29: Single-tone FFT with F_{IN} = 5 MHz,
F_S = 90 MHz, A_{IN} = –1 dBFS

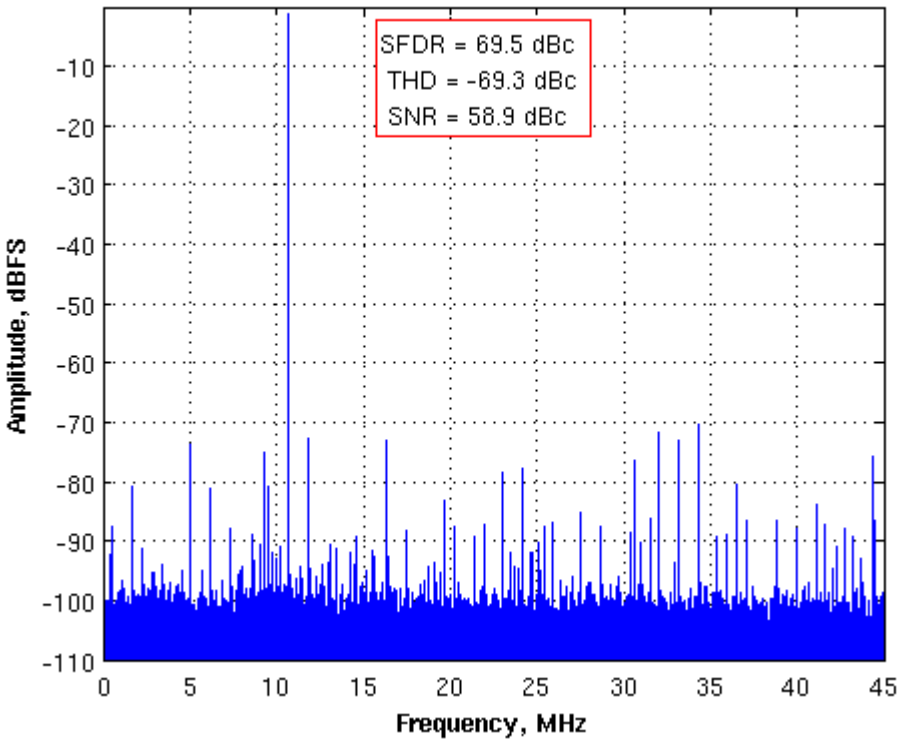

Figure 30: Single-tone FFT with F_{IN} = 10.7 MHz,
F_S = 90 MHz, A_{IN} = –1 dBFS

11 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Layout or blackbox
- Verilog, lef and lib files
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.0:

- Section 1 was changed
- Section 8 shifted to section 9
- Section 8 was added
- Subsection 9.1 was changed
- Subsection 9.2 was changed
- Subsection 9.3 was changed