50 MSPS 2-bit 2-channel special ADC

SPECIFICATION

1 FEATURES

- UMC CMOS 180 nm
- Resolution 2 bit
- 2-channel
- Adjustment of threshold levels
- Adjustment of dc level of thresholds scale
- Analog supply voltage – 3.3 V; digital supply voltage – 1.8 V
- Supported foundries: TSMC, Global Foundries, SMIC, iHP, Vanguard, SilTerra

2 APPLICATION

- Correlators
- Special processors in navigation systems
- AGS systems

3 OVERVIEW

The circuit is 2-bit ADC with programmable threshold. Least significant bit, calling sign bit, turns to 1 or 0 with changing of differential input signal's polarity. Most significant bit, calling magnitude bit, turns to 1 if there is an excess of the threshold by differential input signal.
The block consists of reference voltages and currents generator, 2 voltage followers, 2 ADCs (for each channel) and multiplexers of input signal.
Thresholds are choosed by external 4-bit binary code in range from 60 mV to 220 mV. Threshold's step equals 10 mV. There is two modes to define the threshold: «12 levels» mode and «16 levels» mode. Shifting between these modes is adjusted by logical level at lvl_12_mode input: logical "1" for «12 levels» mode; logical "0" for «16 levels» mode. There is a possibility to adjust the dc level of thresholds' scale within 10 mV, wherein quantizing step remains unchangeable. Scale adjustment implemented by binary code at input scale_adj. Scale adjustment affects both channels at the same time.
There is logical error detector in ADC. In case of appearance one of faulty decisions logical level at the error output of corresponding channel. The faulty decisions are:

- Simultaneous signal of negative sign and upper threshold crossing
- Simultaneous signal of positive sign and lower threshold crossing
- Simultaneous signal of both upper and lower thresholds crossing

The block is designed on UMC CMOS 180 nm technology.

4 STRUCTURE

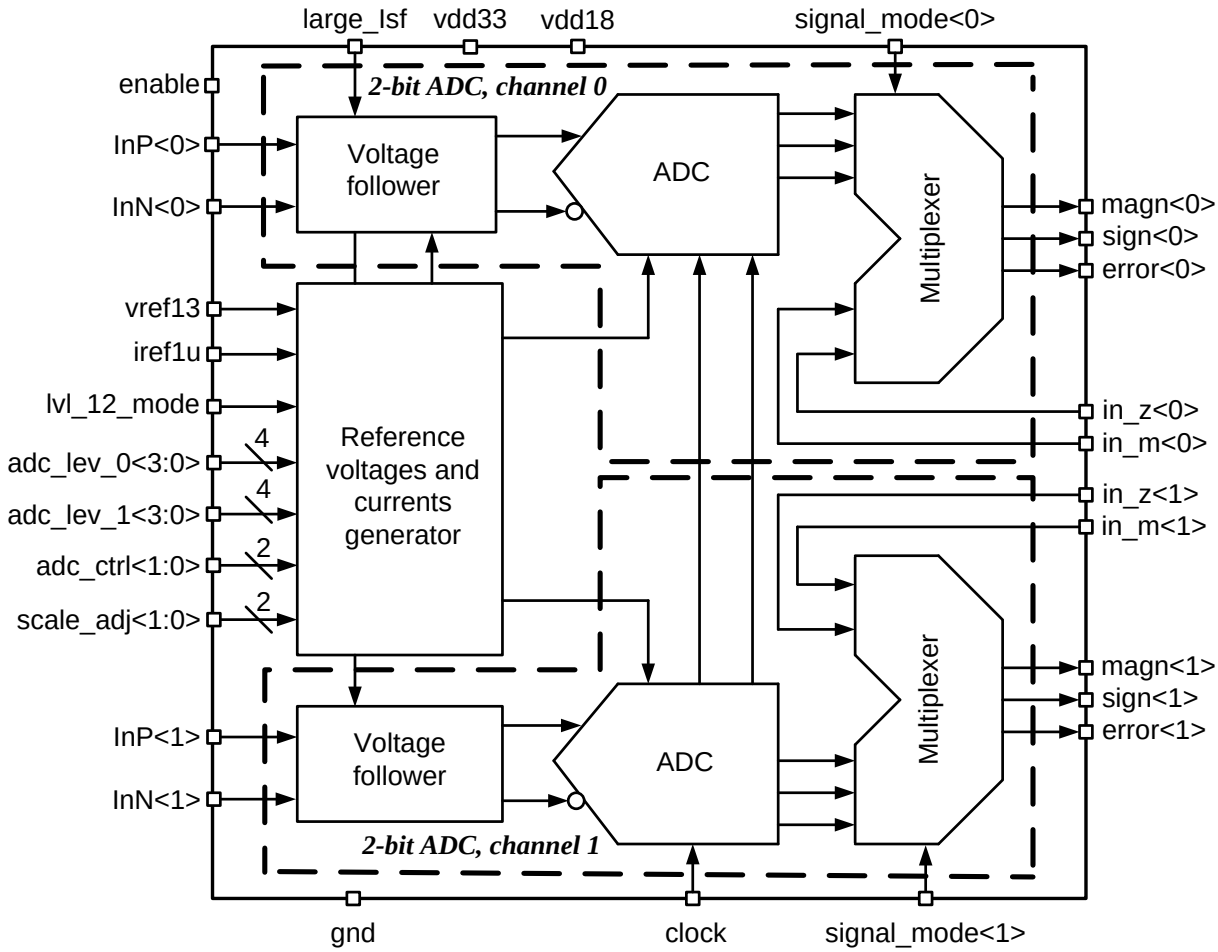

Figure 1: 50 MSPS 2-bit 2-channel special ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
iref1u	I	Reference current 1 uA (influent)
verf13	I	Reference voltage 1.3 V
clock	I	Clock input
enable	I	Enable of device
lvl_12_mode	I	«12/16 levels» mode switch
large_Isf	I	Large voltage followers' current mode enable
adc_ctrl<1:0>	I	Clock enable (for each channel)
InP<1:0>	I	Analog differential input (for each channel)
InN<1:0>		
adc_lev_0<3:0>	I	Tune of threshold in channel 0
adc_lev_1<3:0>	I	Tune of threshold in channel 1
in_m<1:0>	I	Digital input for magnitude signal (for each channel)
in_z<1:0>	I	Digital input for sign signal (for each channel)
signal_mode<1:0>	I	Switch of output signal source (for each channel)
scale_adj<1:0>	I	Thresholds' scale dc level adjustment
magn<1:0>	O	Signal of excess of threshold by input signal (for each channel)
sign<1:0>	O	Sign signal (for each channel)
error<1:0>	O	Error signal (for each channel)
vdd33	IO	Analog supply voltage 3.3 V
vdd18	IO	Digital supply voltage 1.8 V
gnd	IO	Ground voltage

6 LAYOUT DESRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	243	um
Width	218	um

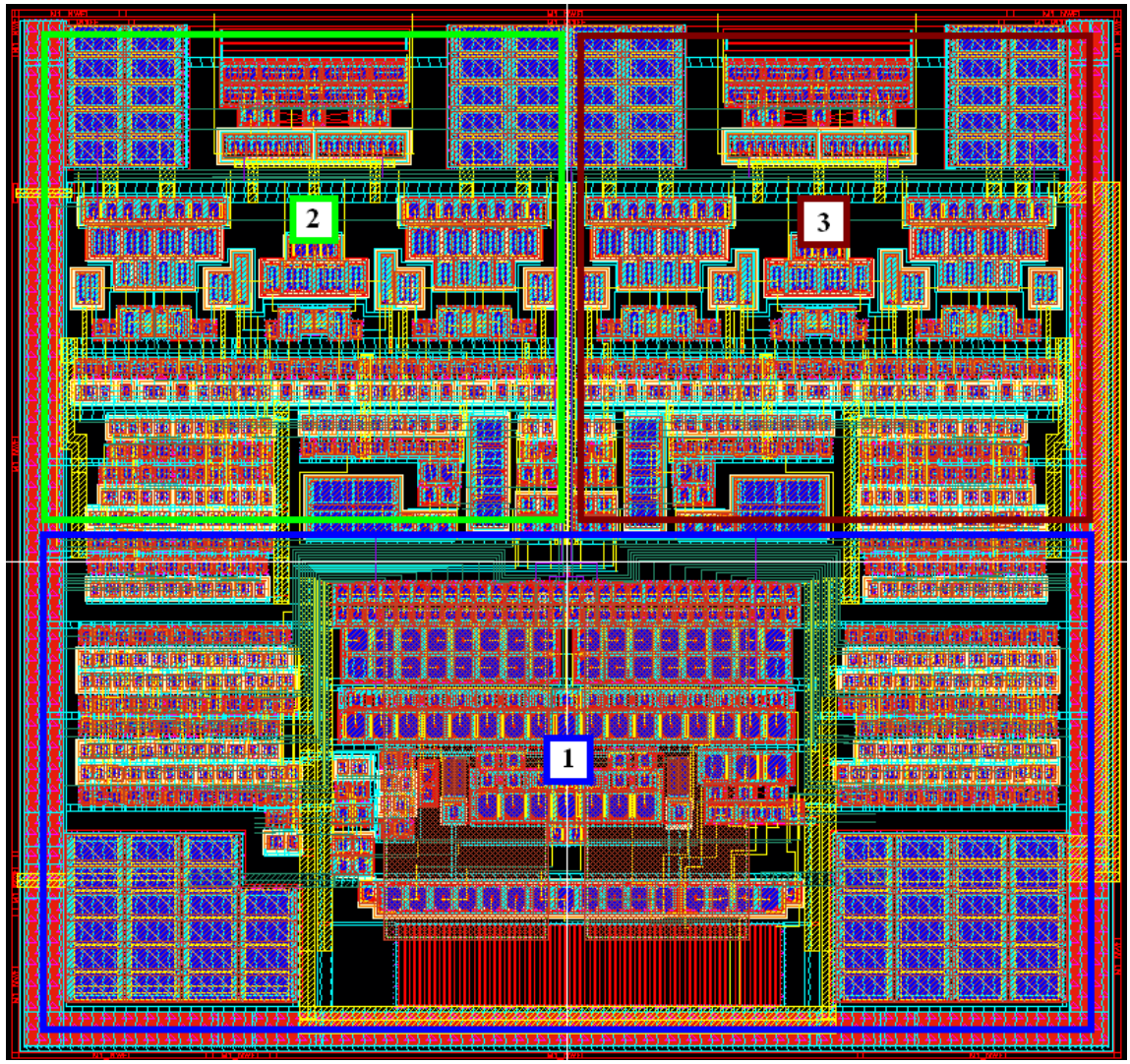

Figure 2: Layout 50 MSPS 2-bit 2-channel special ADC

1. Reference voltages and currents generator
2. 2-bit ADC, channel 0
3. 2-bit ADC, channel 1

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ UMC CMOS 180 nm
Status _____ silicon proven
Total area _____ 0.053 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd18} = 1.7 ÷ 1.9 V, V_{dd33} =3.0 ÷ 3.6 V, T_j = -45 ÷ +85 °C. Typical values are at V_{dd18} = 1.8 V, V_{dd33} = 3.3 V, T_j = +27°C, unless otherwise noted.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Digital supply voltage	V_{dd18}	-	1.7	1.8	1.9	V
Analog supply voltage	V_{dd33}	-	3	3.3	3.6	V
Operating temperature	T_j	-	-45	27	+85	°C
Resolution	N	-	2	-	-	bit
Clock frequency	F_{clk}	-	50	-	100	MHz
Sampling rate	F_S	-	-	50	-	MSPS
Bandwidth	BW	-	25	-	50	MHz
Standby power	P_{st}	-	0.016	29.1	-	uW
Digital blocks supply current	$I_{supply18}$	-	-	704.3	-	uA
Analog blocks supply current	$I_{supply33}$	2 channels	-	1422.3	-	uA
Total power	P_{total}	-	-	5.97	-	mW
DC level of input signal	U	-	1.5	1.7	1.9	V
Input high-logic level	V_{IH}	For digital inputs	$0.7V_{cc}$	-	V_{cc}+0.25	V
Input low-logic level	V_{IL}		-0.25	-	$0.3V_{cc}$	V

8 TYPICAL CHARACTERISTICS

In tables: p3: magn = 1, sign = 1; p1: magn = 0, sign = 1; m1: magn = 0, sign = 0; m3: magn = 1, sign = 1

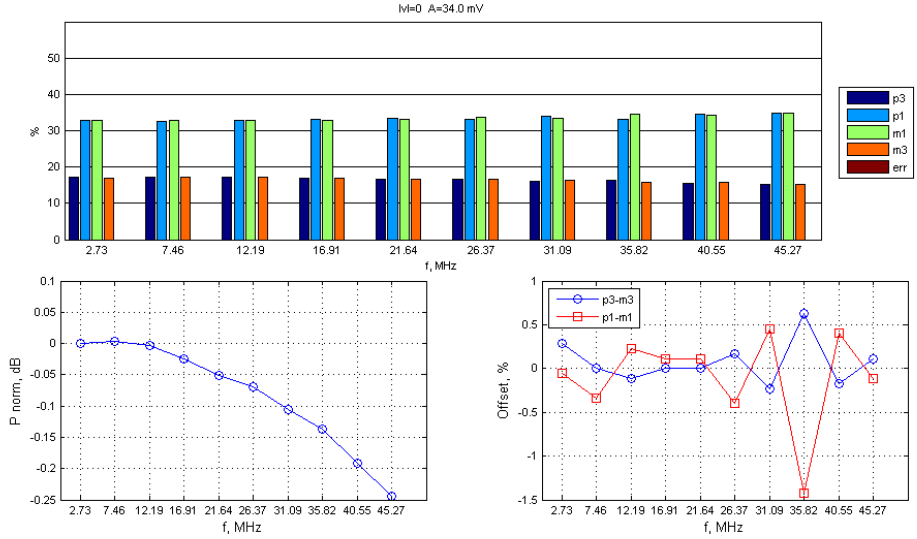

Figure 3: Results of parametrical analysis for sine input signal at different frequencies and amplitude of 34 mV. Threshold №1

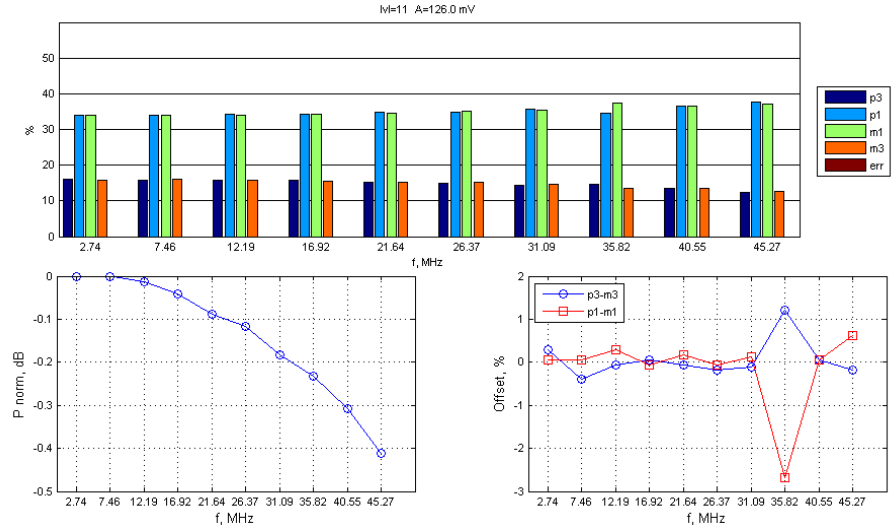

Figure 4: Results of parametrical analysis for sine input signal at different frequencies and amplitude of 126 mV. Threshold №12

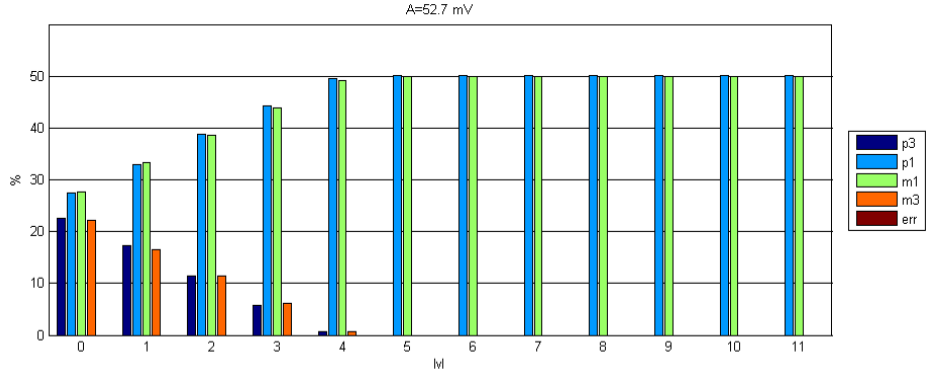

Figure 5: Results of parametrical analysis for random input signal. Magnitude is 52.7 mV. At different thresholds

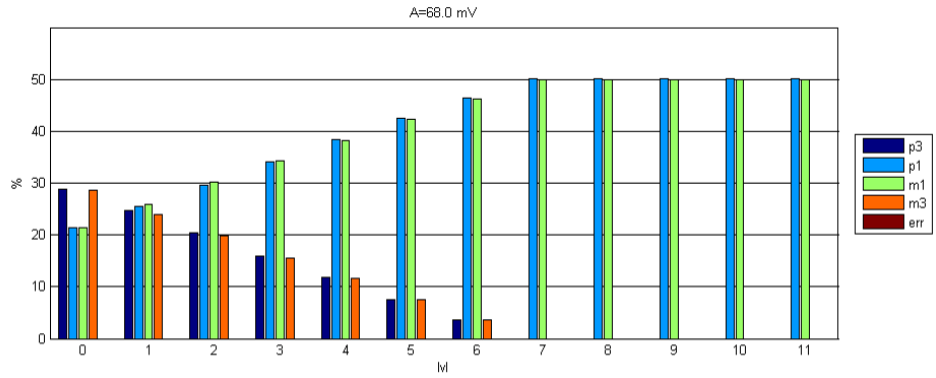

Figure 6: Results of parametrical analysis for random input signal. Magnitude is 68 mV. At different thresholds

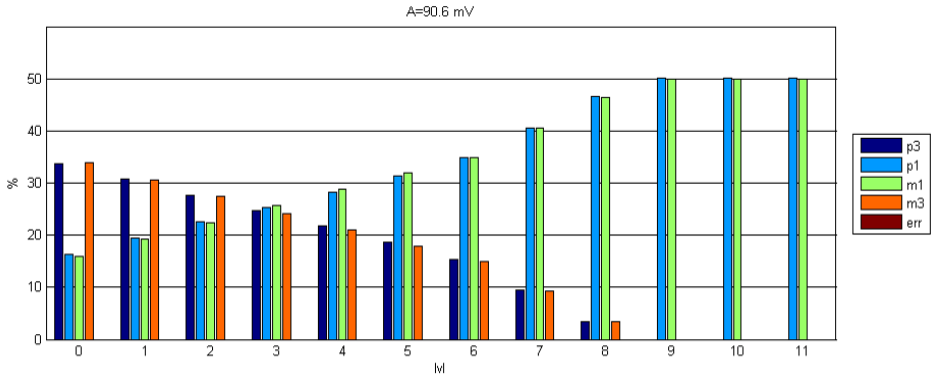

Figure 7: Results of parametrical analysis for random input signal. Magnitude is 90.6 mV. At different thresholds

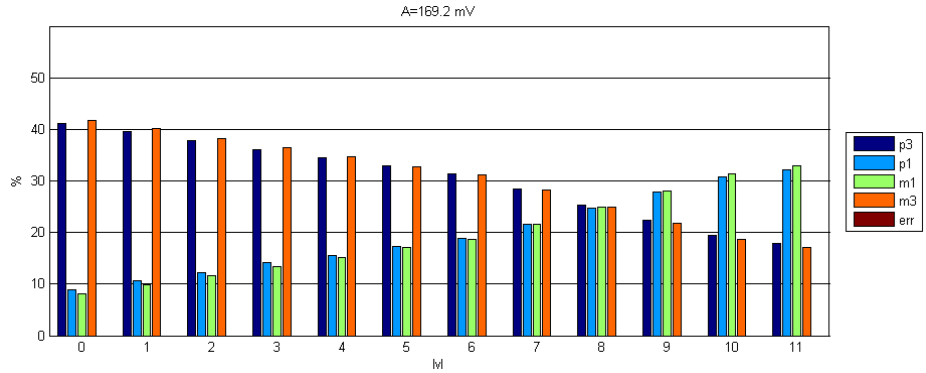

Figure 8: Results of parametrical analysis for random input signal. Magnitude is 169.2 mV. At different thresholds

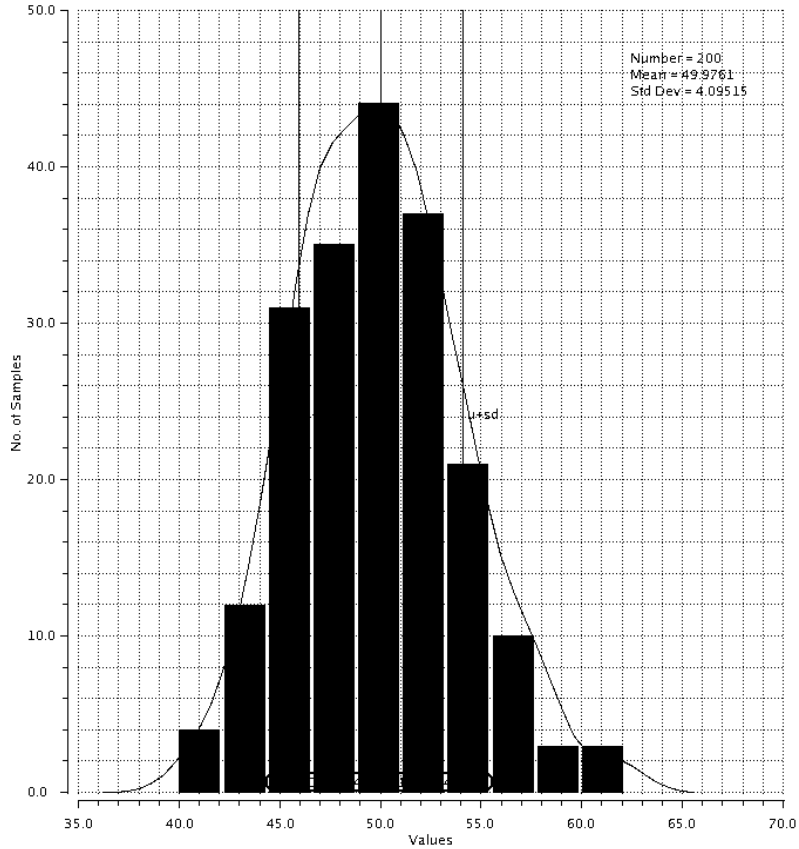

Figure 9: Results of Monte Carlo simulation by logical “1” filling at sign output. Sine input signal

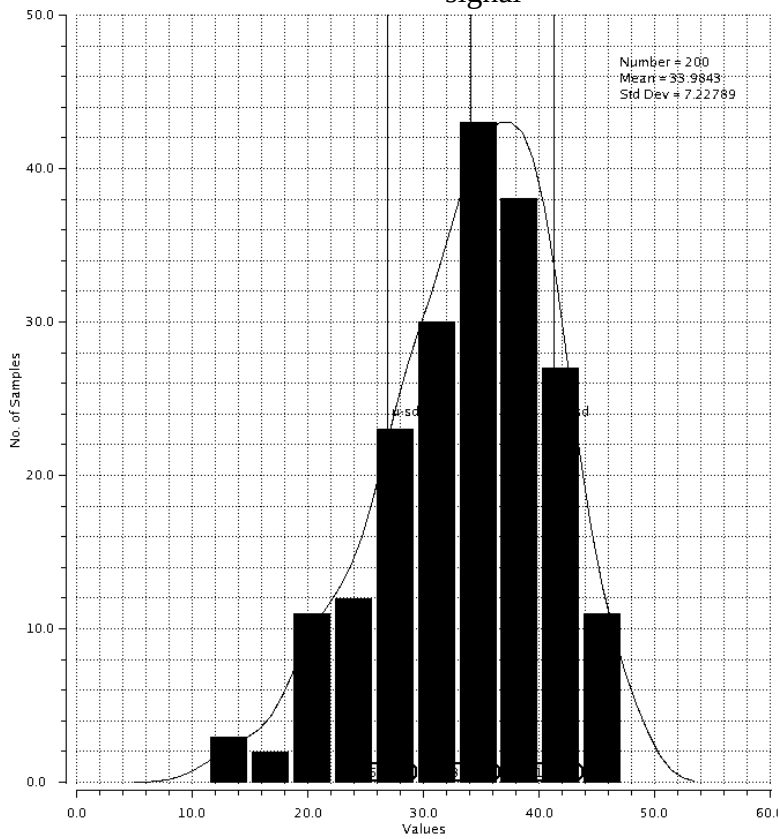

Figure 10: Results of Monte Carlo simulation by logical “1” filling at magn output. Sine input signal. Amplitude 34 mV; threshold №0

9 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation