12-bit 2-channel 2.18 MSPS delta-sigma ADC

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Low current consumption
- Operating frequency range of 0…8.5 kHz
- Oversampling ratio 128
- No external components required
- Small area
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, Vanguard, SilTerra

2 APPLICATION

- Receivers, transmitters, transceivers
- Analog integrated circuits

3 OVERVIEW

The cell is a second order delta-sigma 2-channel (I/Q) analog-to-digital converter that supports sample rates up to 8.5 kHz and oversampling ratio 128. This structure is based on the principle of switch capacitors and consists of two differential channels.
The block is designed on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

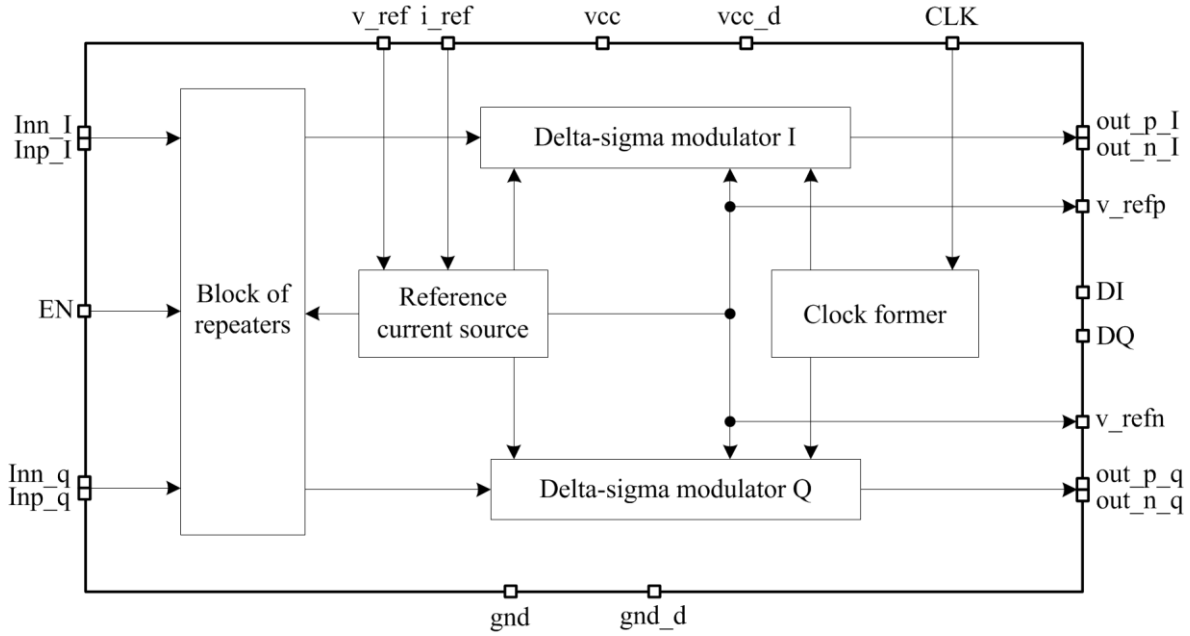

Figure 1: 12-bit 2-channel 2.18 MSPS delta-sigma ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
i_ref	I	Reference current 10 uA
v_ref	I	Reference voltage
Inn_I	I	I channel analog differential input
Inp_I	I	
Inn_q	I	Q channel analog differential input
Inp_q	I	
CLK	I	CMOS input clock (~ 2.5 MHz)
EN	I	Enable/disable ADC
out_p_I	O	I channel CMOS single-bit output
out_q_I	O	
out_p_q	O	Q channel CMOS single-bit output
out_n_q	O	
DI	O	I channel digital output
DQ	O	Q channel digital output
v_refp	IO	Reference voltage differential input matched to an input reference voltage source
v_refn	IO	
vcc_d	IO	Digital supply voltage 2.2 V
vcc	IO	Supply voltage 2.2 V
gnd_d	IO	Digital ground
gnd	IO	Ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	597	um
Width	817	um

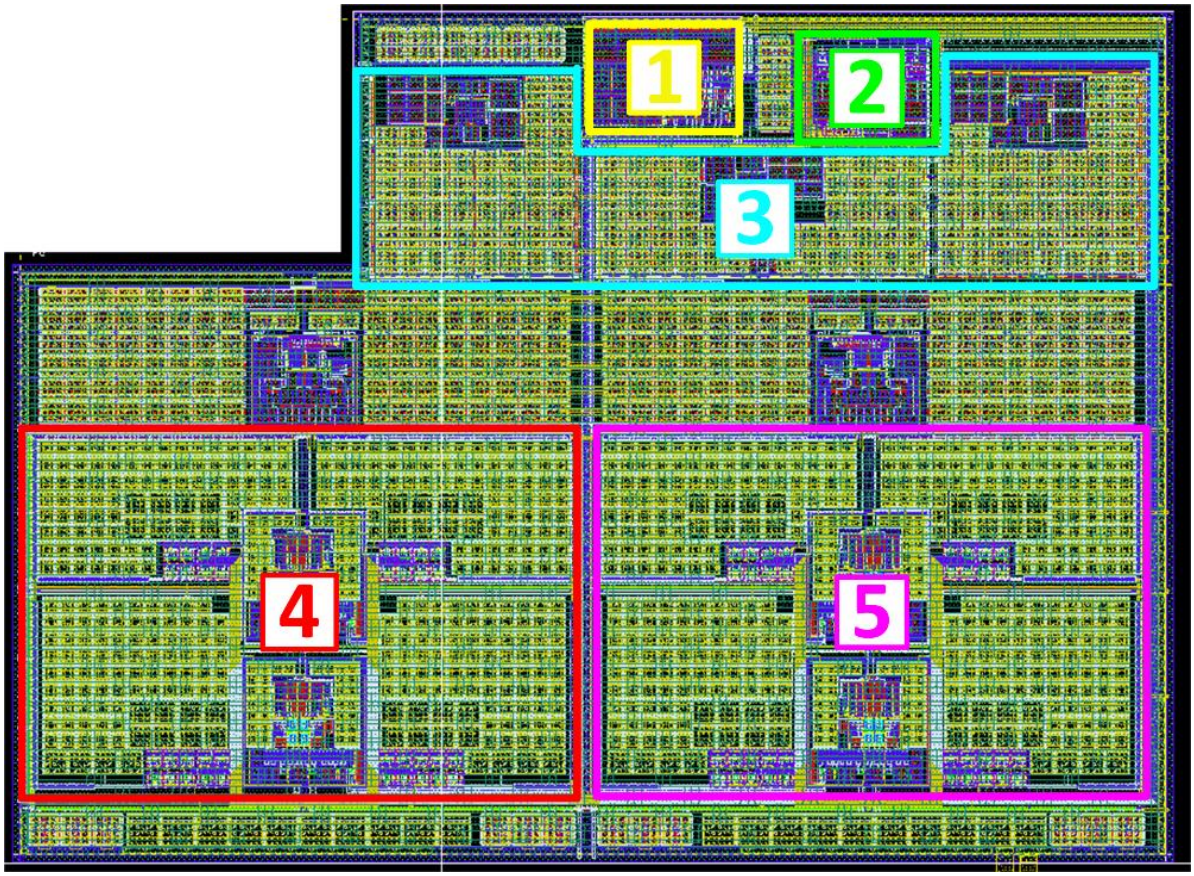

Figure 2: Layout 12-bit 2-channel 2.18 MSPS delta-sigma ADC

1. Reference current source
2. Clock former
3. Block of repeaters
4. Delta-sigma modulator I
5. Delta-sigma modulator Q

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
Status _____ silicon proven
Area _____ 0.49 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{cc} = V_{CCdig} = 1.7 \div 2.3$ V and $T_j = -45 \div +85$ °C. Typical values are at $V_{cc} = V_{CCdig} = 2.2$ V, $T_j = +27$ °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{CC}	-	1.7	2.2	2.3	V
Digital supply voltage	V_{CCdig}	-	1.7	2.2	2.3	V
Operating temperature range	T	-	-40	27	+85	°C
Resolution	N	-	-	12	-	bit
Input signal frequency	F_{IN}	-	0.0	-	8.5	kHz
Bandwidth	BW	-	-	8.5	-	kHz
Sampling rate	F_s	-	-	2.2	-	MSPS
Input reference voltage	V_{REF+}	-	1.18	1.29	1.37	V
	V_{REF-}		0.86	0.96	1.05	V
Peak-to-peak differential input voltage	$A_{in\ p-p}$	-	560	-	640	mV
DC operating point	U	-	1.05	1.134	1.250	V
Signal - noise ratio	SNR	With an amplitude closed to the maximum (2.5 dB)	-	62	-	dB
Dynamic range	SFDR	-	-	50	-	dB
Noise figure	P_{NOISE}	In the bandwidth with full amplitude ($V_{REF+} - V_{REF-}$)	-	-53	-	dB
Intermodulation immunity*	α_{IM}	Limited by SNR, there is no intermodulation peak	62	-	-	dB
Current consumption	I_{CC}	For one channel	430	450	455	uA
Input logic-high level	V_{IH}	For digital inputs	$0.7V_{CC}$	-	$V_{CC}+0.25$	V
Input logic-low level	V_{IL}		-0.25	-	0.3	V

*Two tones are located at 20 kHz and 35 kHz offset frequencies from the centre frequency of 5 kHz.

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Layout or blackbox
- Verilog, lef and lib files
- Extracted view (optional)
- HDL-description of digital filters
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.2:

- Subsection 7.1 updated

From version 1.1:

- Subsection 7.2 updated