12-bit 1-channel 10 to 100 MSPS pipeline ADC

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Resolution 12 bit
- Sampling frequency 10 to 100 MHz
- Low power consumption in standby model
- Low power dissipation (150 mW)
- Spurious-free dynamic range (SFDR) 62 dB
- Signal-to-noise ratio (SNR) 61 dB
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, SilTerra

2 APPLICATION

- Optical networking
- Test equipment
- Portable ultrasound and digital beam-forming systems
- Telecommunication systems
- Higher quality imaging in video systems

3 OVERVIEW

The low-power high-speed 12-bit ADC employs high-performance differential pipeline architecture.

The ADC consists of a sample and hold device, a core ADC and block of comparators. The ADC requires: 2.5 V analog supply, differential reference voltages 1.5 V and 1.0 V, common mode voltage 0.75 V and differential input clock.

The ADC supports standby mode which allows state with minimum power consumption.

There is also the ability to configure the operating modes of the ADC by using digital registers.

The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.
4 STRUCTURE

Figure 1: 12-bit 1-channel 10 to 100 MSPS pipeline ADC structure
## 5 PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Name</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>rp</td>
<td>I</td>
<td>High level reference voltage 1.5 V</td>
</tr>
<tr>
<td>rm</td>
<td>I</td>
<td>Low level reference voltage 1 V</td>
</tr>
<tr>
<td>ip</td>
<td>I</td>
<td>Analog differential input</td>
</tr>
<tr>
<td>in</td>
<td></td>
<td></td>
</tr>
<tr>
<td>clkp</td>
<td>I</td>
<td>Differential input clock signal</td>
</tr>
<tr>
<td>clkn</td>
<td>I</td>
<td></td>
</tr>
<tr>
<td>cm</td>
<td>I</td>
<td>Average level of the reference voltage</td>
</tr>
<tr>
<td>cmc</td>
<td>I</td>
<td>Reference level for comparators</td>
</tr>
<tr>
<td>boost</td>
<td>I</td>
<td>Reference level for keys block</td>
</tr>
<tr>
<td>bp</td>
<td>I</td>
<td>Reference level for current sources</td>
</tr>
<tr>
<td>bpc</td>
<td>I</td>
<td>Reference level for current sources</td>
</tr>
<tr>
<td>bn</td>
<td>I</td>
<td>Reference level for current sources</td>
</tr>
<tr>
<td>clk_out</td>
<td>O</td>
<td>Output clk signal</td>
</tr>
<tr>
<td>rng&lt;4:0&gt;</td>
<td>I</td>
<td>Comparators selection register(1/8 or 3/8)</td>
</tr>
<tr>
<td>dout&lt;11:0&gt;</td>
<td>O</td>
<td>Output data signal</td>
</tr>
<tr>
<td>vdd</td>
<td>I/O</td>
<td>Supply voltage 2.5 V</td>
</tr>
<tr>
<td>gnd</td>
<td>I/O</td>
<td>Ground bus</td>
</tr>
</tbody>
</table>
6 LAYOUT DESCRIPTION

Analog-to-digital converter layout dimensions are given in the table 1.

Table 1: Block dimensions of the 12-bit ADC

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Height</td>
<td>1725</td>
<td>um</td>
</tr>
<tr>
<td>Width</td>
<td>660</td>
<td>um</td>
</tr>
</tbody>
</table>

Figure 2: 12-bit 1-channel 10 to 100 MSPS pipeline ADC layout

1. Sample and hold device
2. Block of ADC core
3. Flash ADC
7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology______________________________iHP SiGe BiCMOS 0.25 um
Status______________________________silicon proven
Area______________________________1.14 mm²

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for \( V_{dd} = 2.25 \div 2.75 \) V, \( T_j = -60 \div +125 \) °C. Typical values are \( V_{dd} = 2.5 \) V, \( T_j = +27 \) °C, unless otherwise specified.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Unit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>( V_{dd} )</td>
<td>-</td>
<td>V</td>
<td>2.25 - 2.75</td>
</tr>
<tr>
<td>Operating temperature range</td>
<td>( T_j )</td>
<td>-</td>
<td>°C</td>
<td>-60 - 125</td>
</tr>
<tr>
<td>Resolution</td>
<td>N</td>
<td>-</td>
<td>Bit</td>
<td>1 - 12</td>
</tr>
<tr>
<td>Maximum input amplitude</td>
<td>( A_{IN} )</td>
<td>-</td>
<td>V</td>
<td>0.5</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>BW</td>
<td>-</td>
<td>MHz</td>
<td>5 - 50</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>( F_s )</td>
<td>-</td>
<td>MSPS</td>
<td>10 - 100</td>
</tr>
<tr>
<td>Input reference voltage</td>
<td>( V_{REF+} ), ( V_{REF-} )</td>
<td>-</td>
<td>V</td>
<td>1.5 - 1</td>
</tr>
<tr>
<td>Peak-to-peak differential input voltage</td>
<td>( A_{IN_{pp}} )</td>
<td>-</td>
<td>V</td>
<td>1 - 1</td>
</tr>
<tr>
<td>DC operating point</td>
<td>U</td>
<td>-</td>
<td>V</td>
<td>0.5 ( V_{dd} ) - 100 mV, 0.5 ( V_{dd} ) + 100 mV</td>
</tr>
<tr>
<td>Signal-to-noise ratio</td>
<td>SNR</td>
<td>-</td>
<td>dB</td>
<td>61 - 64</td>
</tr>
<tr>
<td>Spurious-free dynamic range</td>
<td>SFDR</td>
<td>-</td>
<td>dB</td>
<td>56 - 62 - 64</td>
</tr>
<tr>
<td>Standby current</td>
<td>( I_{st} )</td>
<td>-</td>
<td>uA</td>
<td>60 - 60</td>
</tr>
<tr>
<td>Current consumption</td>
<td>( I_{cc} )</td>
<td>-</td>
<td>mA</td>
<td>60 - 60</td>
</tr>
<tr>
<td>Input high-logic level</td>
<td>( V_{HI} )</td>
<td>For digital inputs</td>
<td>V</td>
<td>( 0.7 V_{dd} ) - ( V_{dd} + 0.25 )</td>
</tr>
<tr>
<td>Input low-logic level</td>
<td>( V_{IL} )</td>
<td>-</td>
<td>V</td>
<td>-0.25 - 0.3</td>
</tr>
</tbody>
</table>

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation
REVISION HISTORY

From version 1.2:
- Section 4 updated
- Section 6 updated
- Subsection 7.1 updated

From version 1.1:
- Section 3 updated
- Section 4 updated
- Subsection 7.2 updated