12-bit 1-channel 10 to 100 MSPS pipeline ADC

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Resolution 12 bit
- Sampling frequency 10 to 100 MHz
- Low power consumption in standby model
- Low power dissipation (150 mW)
- Spurious-free dynamic range (SFDR) 62 dB
- Signal-to-noise ratio (SNR) 61 dB
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, SilTerra

2 APPLICATION

- Optical networking
- Test equipment
- Portable ultrasound and digital beam-forming systems
- Telecommunication systems
- Higher quality imaging in video systems

3 OVERVIEW

The low-power high-speed 12-bit ADC employs high-performance differential pipeline architecture.
The ADC consists of a sample and hold device, a core ADC and block of comparators. The ADC requires: 2.5 V analog supply, differential reference voltages 1.5 V and 1.0 V, common mode voltage 0.75 V and differential input clock.
The ADC supports standby mode which allows state with minimum power consumption.
There is also the ability to configure the operating modes of the ADC by using digital registers.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

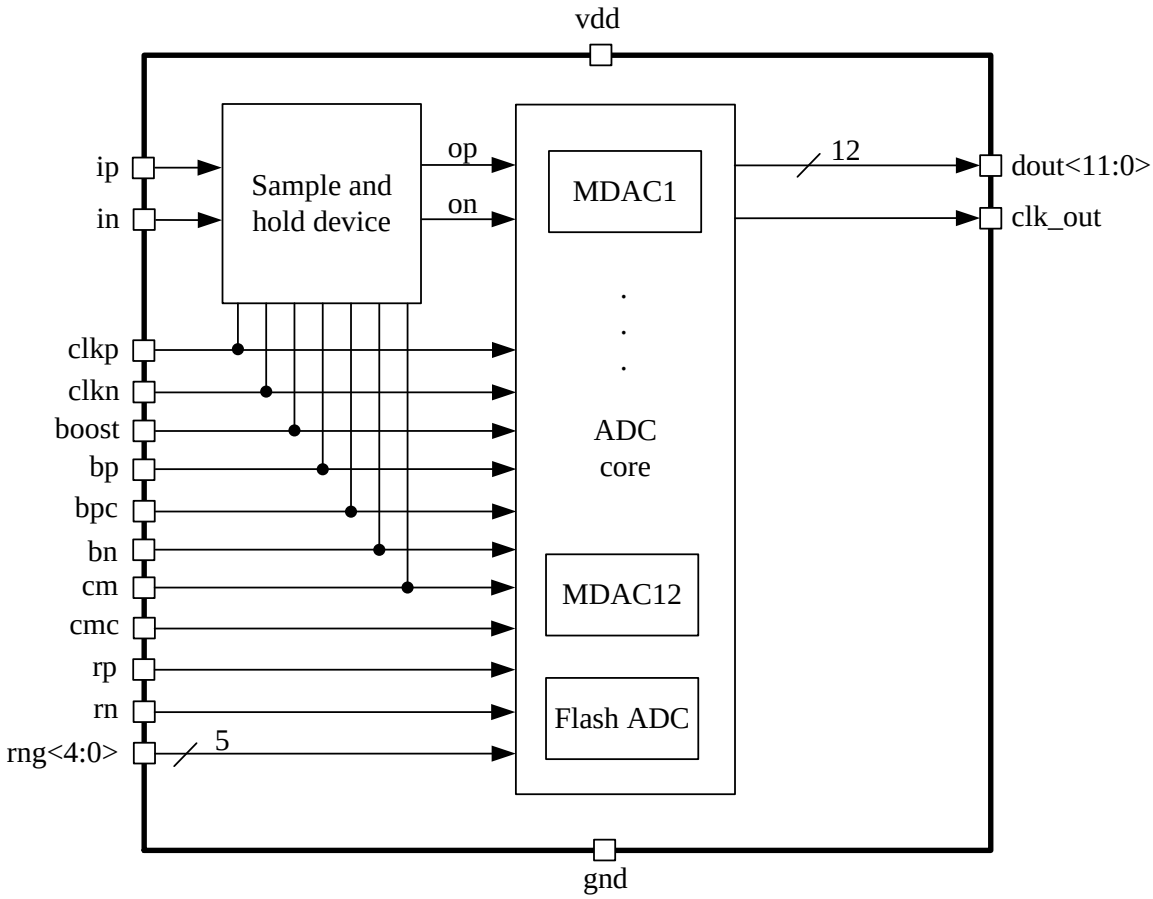

Figure 1: 12-bit 1-channel 10 to 100 MSPS pipeline ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
rp	I	High level reference voltage 1.5 V
rn	I	Low level reference voltage 1 V
ip	I	Analog differential input
in		
clkp	I	Differential input clock signal
clkn		
cm	I	Average level of the reference voltage
cmc	I	Reference level for comparators
boost	I	Reference level for keys block
bp	I	Reference level for current sources
bpc	I	Reference level for current sources
bn	I	Reference level for current sources
clk_out	O	Output clk signal
rng<4:0>	I	Comparators selection register(1/8 or 3/8)
dout<11:0>	O	Output data signal
vdd	I/O	Supply voltage 2.5 V
gnd	I/O	Ground bus

6 LAYOUT DESCRIPTION

Analog-to-digital converter layout dimensions are given in the table 1.

Table 1: Block dimensions of the 12-bit ADC

Dimension	Value	Unit
Height	1725	um
Width	660	um

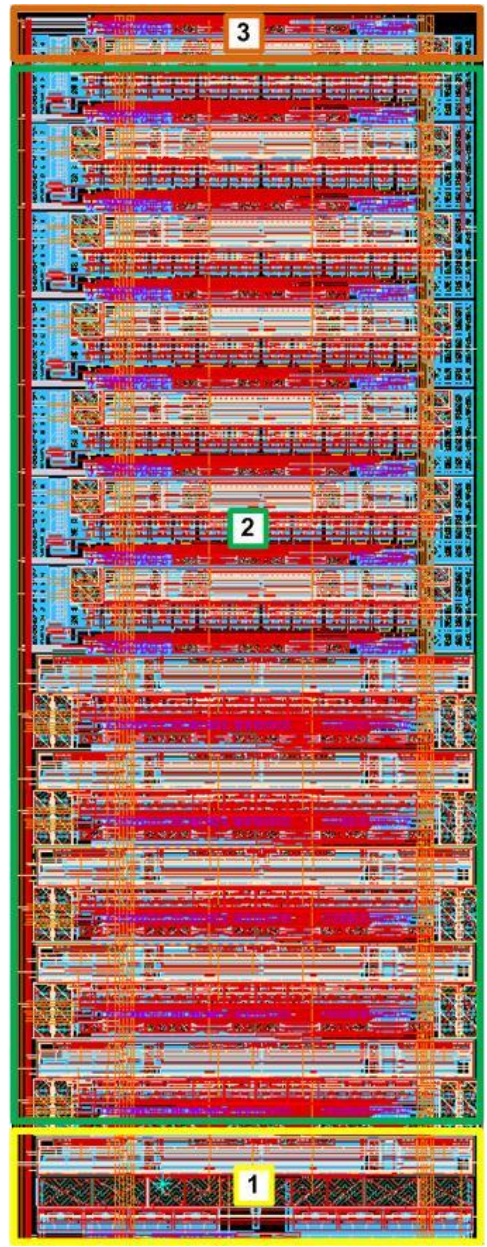

Figure 2: 12-bit 1-channel 10 to 100 MSPS pipeline ADC layout

1. Sample and hold device
2. Block of ADC core
3. Flash ADC

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology iHP SiGe BiCMOS 0.25 um
Status silicon proven
Area 1.14 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd} = 2.25 ÷ 2.75 V, T_j = -60 ÷ +125 °C. Typical values are V_{dd} = 2.5 V, T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{dd}	-	2.25	2.5	2.75	V
Operating temperature range	T_j	-	-60	27	+125	°C
Resolution	N	-	-	12	-	Bit
Maximum input amplitude	A_{IN}	-	-	0.5	-	V
Bandwidth	BW	-	5	-	50	MHz
Sampling rate	F_s	-	10	-	100	MSPS
Input reference voltage	V_{REF+}	-	-	1.5	-	V
	V_{REF-}		-	1	-	V
Peak-to-peak differential input voltage	$A_{IN\ p-p}$	-	-	1	-	V
DC operating point	U	-	$0.5V_{dd}$ -100 mV	$0.5V_{dd}$	$0.5V_{dd}$ +100 mV	V
Signal-to-noise ratio	SNR	Input amplitude $0.9A_{IN}$, input frequency 10.7 MHz, F_{clk} = 50 MHz	-	61	-	dB
Spurious-free dynamic range	SFDR		56	62	64	dB
Standby current	I_{st}	-	-	60	-	uA
Current consumption	I_{cc}	-	-	60	-	mA
Input high-logic level	V_{IH}	For digital inputs	$0.7V_{dd}$	-	V_{dd}+0.25	V
Input low-logic level	V_{IL}		-0.25	-	0.3	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.2:

- Section 4 updated
- Section 6 updated
- Subsection 7.1 updated

From version 1.1:

- Section 3 updated
- Section 4 updated
- Subsection 7.2 updated