

# 12-bit 1-channel 25 MSPS pipeline ADC

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## SPECIFICATION

### 1 FEATURES

- iHP SiGe BiCMOS 0.25  $\mu\text{m}$
- Resolution 12 bit
- Sampling frequency 15 to 25 MHz
- Low power consumption in standby mode
- Low power dissipation (125 mW)
- Signal-to-noise ratio (SNR) 61 dB
- Spurious-free dynamic range (SFDR) 62 dB
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, AMS, SilTerra, X-FAB

### 2 APPLICATION

- Optical networking
- Test equipment
- Portable ultrasound and digital beam-forming systems
- Telecommunication systems
- Higher quality imaging in video systems

### 3 OVERVIEW

The low-power high-speed 12-bit ADC employs high-performance differential pipeline architecture.

The ADC consists of a sample and hold device, a core ADC and block of comparators. The ADC requires: 2.5 V analog supply, differential reference voltages 1.5 V and 1.0 V, common mode voltage 0.75 V and differential input clock.

The ADC supports standby mode which allows state with minimum power consumption.

There is also the ability to configure the operating modes of the ADC by using digital registers.

The block is fabricated on iHP SiGe BiCMOS 0.25  $\mu\text{m}$  technology.

## 4 STRUCTURE

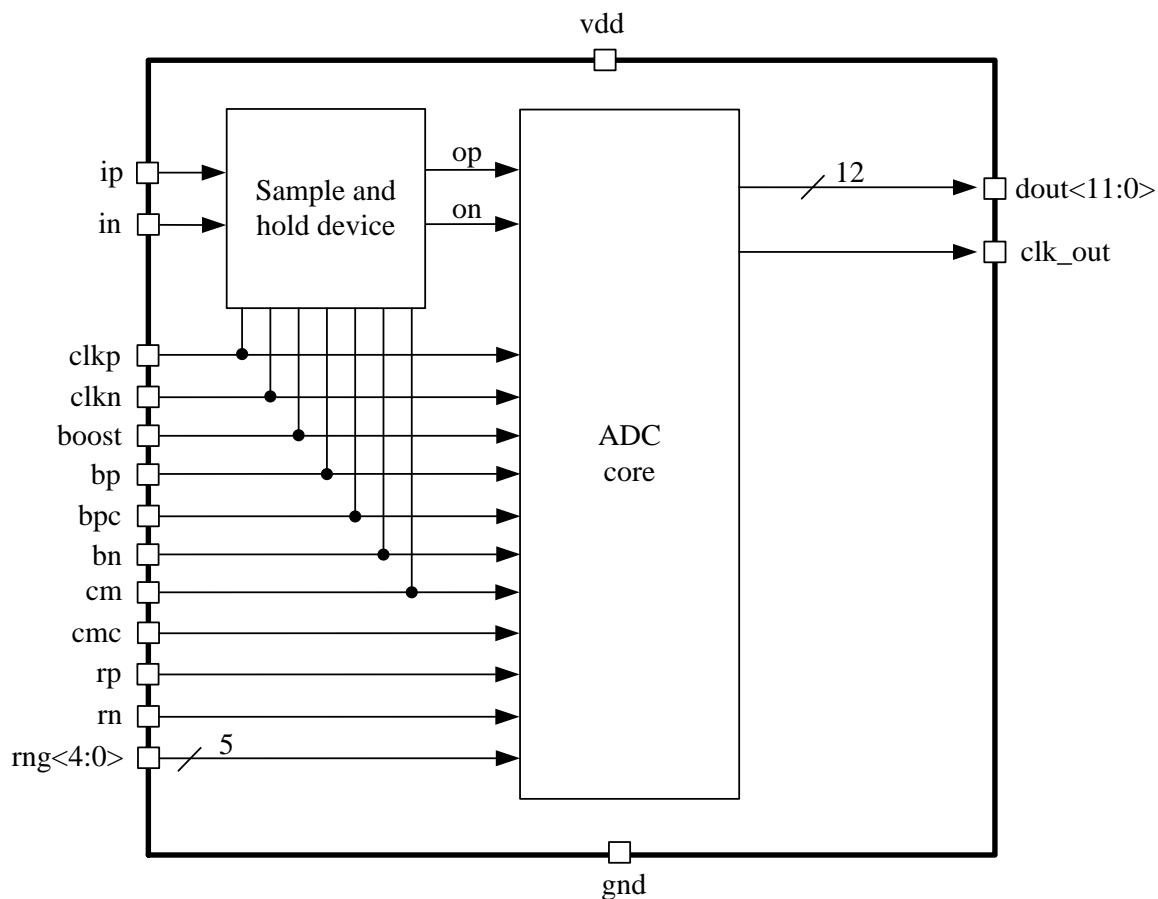


Figure 1: 12-bit 1-channel 25 MSPS pipeline ADC structure

## 5 PIN DESCRIPTION

Name	Direction	Description
ip	I	Analog differential input
in		
clkp	I	Differential input clock signal
clkn		
boost	I	Reference level for keys block
bp	I	Reference level for current sources
bpc	I	Reference level for current sources
bn	I	Reference level for current sources
cm	I	Average level of the reference voltage
cmc	I	Reference level for comparators
rp	I	High level reference voltage
rn	I	Low level reference voltage
rng<4:0>	I	Comparators selection register (1/8 or 3/8)
dout<11:0>	O	Output data signal
clk_out	O	Output clk signal
vdd	I/O	Supply voltage 2.5 V
gnd	I/O	Ground bus

## 6 LAYOUT DESCRIPTION

Analog-to-digital converter layout dimensions are given in the table 1.

**Table 1:** Block dimensions of the 12-bit ADC

Dimension	Value	Unit
Height	2280	$\mu\text{m}$
Width	340	$\mu\text{m}$

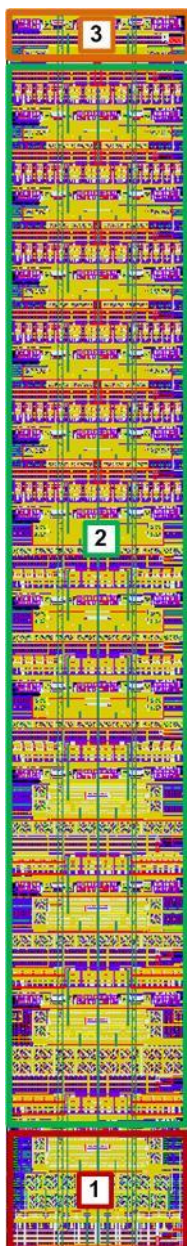


Figure 2: 12-bit ADC layout view

1. Sample and hold device
2. Block of multiplying DACs
3. Block of comparators

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ iHP SiGe BiCMOS 0.25 um  
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_ 0.8 mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{dd} = 2.25 \div 2.75V$ ,  $T = -60 \div +125^{\circ}C$ . Typical values are  $V_{dd} = 2.5V$ ,  $T = +27^{\circ}C$ , unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	$V_{dd}$	-	2.25	2.5	2.75	V
Operating temperature range	T	-	-60	27	+125	$^{\circ}C$
Resolution	N	-	-	12	-	bit
Standby current	$I_{st}$	-	-	60	-	$\mu A$
Current consumption	$I_{cc}$	-	-	50	-	mA
Maximum input amplitude	$A_{IN}$	-	-	0.5	-	V
Bandwidth	B	-	7.5	10.0	12.5	MHz
Sampling rate	$F_s$	-	15	20	25	MSPS
Input reference voltage	$V_{REF+}$	-	-	1.5	-	V
	$V_{REF-}$		-	1	-	V
Peak-to-peak differential input voltage	$A_{IN\ p-p}$	-	-	1	-	V
DC operating point	U	-	$0.5V_{dd}$ -100mV	$0.5V_{dd}$	$0.5V_{dd}$ +100mV	V
Signal-noise ratio	SNR	Input amplitude $0.9 A_{IN}$ , input frequency 1.5 MHz,	-	61	-	dB
Spurious-free dynamic range	SFDR	$F_{clk} = 20$ MHz	56	62	64	dB
Input logic-level high	$V_{IH}$	For digital inputs	$0.7V_{dd}$	-	$V_{dd}+0.25$	V
Input logic-level low	$V_{IL}$		-0.25	-	0.3	V

## 8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

## REVISION HISTORY

From version 1.1:

- Section 1 updated
- Section 3 updated
- Subsection 7.2 updated