12-bit 2-channel 0.5 to 33 MSPS delta-sigma ADC

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- 2-channel wide-band delta-sigma ADC
- Resolution 12 bit
- Information speed modes: 2.4 kBaud – 512 kBaud
- Supply voltage 1.8 V
- Tunable op amps current
- SFDR 63 dB
- SNR 61 dB
- Input differential signal range 1.6 V
- In-built input signal level detection, sign detection
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, AMS, Vanguard, SilTerra

2 APPLICATION

- Analog to digital conversion of wide-band input signal
- Recievers, transmitters, transceivers
- Analog integral circuits
- Measuring equipment
- Medical equipment

3 OVERVIEW

The block is second order delta-sigma ADC with 5-level quantizer. The block consists of:

- Two integrating cascades based on switch capacitors technique (treats both channels)
- 5-level flash-ADC (treats both channels)
- Tunable (6-bit control) clock signal frequency divider
- Clock splitter
- Block of bias currents, tunable (6-bit control)
- Data-weighted averaging (DWA) correction of capacitors mismatch (treats both channels)
- Input signal level detection

Output signal is represented in “thermometer” code. There is a possibility to disable of each channel, frequency divider, block of bias currents, DWA correction. There is an in-built output from frequency divider for clocking digital filters.

Input DC level is 0.9 V; recommended voltage levels for references are 0.9 ± 0.4 V; recommended input signal differential amplitude is 0.64 V; allowable deviation of clock duty cycle: 50 ± 5%.

The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

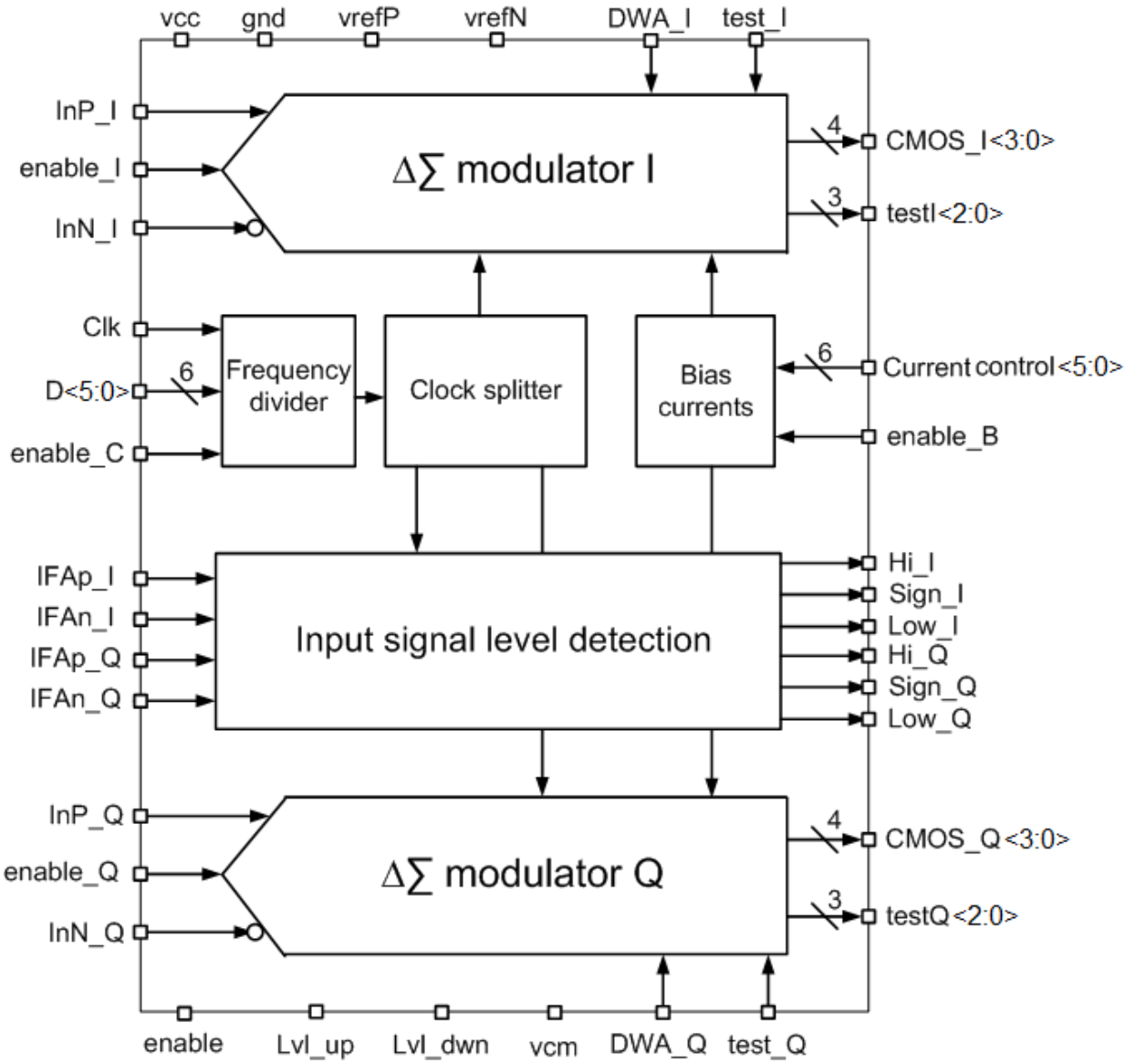

Figure 1: 12-bit 2-channel 0.5 to 33 MSPS delta-sigma ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
enable	I	Enable of device
InP_I	I	Analog differential input of I-channel
InN_I		
enable_I	I	Enable of components of I-channel
DWA_I	I	Enable of DWA of I-channel
test_I	I	Enable of test outputs of I-channel
InP_Q	I	Analog differential input of Q-channel
InN_Q		
enable_Q	I	Enable of components of Q-channel
DWA_Q	I	Enable of DWA of Q-channel
test_Q	I	Enable of test outputs of Q-channel
IFAp_I	I	Differential input of level detector, I channel
IFAn_I		
IFAp_Q	I	Differential input of level detector, Q channel
IFAn_Q		
Lvl_up	I	Differential reference voltage for level detection
Lvl_dwn		
Clk	I	Clock input
enable_C	I	Clock enable
D<5:0>	I	Tune of frequency divider
vrefP	I	Differential reference voltage
vrefN		
vcm	I	Common mode voltage
Current control<5:0>	I	Tune of op amps currents
enable_B	I	Enable of bias currents
CMOS_I<3:0>	O	Digital output, I channel
CMOS_Q<3:0>	O	Digital output, Q channel
testI<2:0>	O	Test digital output, I channel
testQ<2:0>	O	Test digital output, Q channel
Hi_I	O	Excess level by signal, I channel
Sign_I	O	Sign of signal, I channel
Low_I	O	Reduction level by signal, I channel
Hi_Q	O	Excess level by signal, Q channel
Sign_Q	O	Sign of signal, Q channel
Low_Q	O	Reduction level by signal, Q channel
vcc	I/O	Supply voltage
gnd	I/O	Ground voltage

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	465	um
Width	650	um

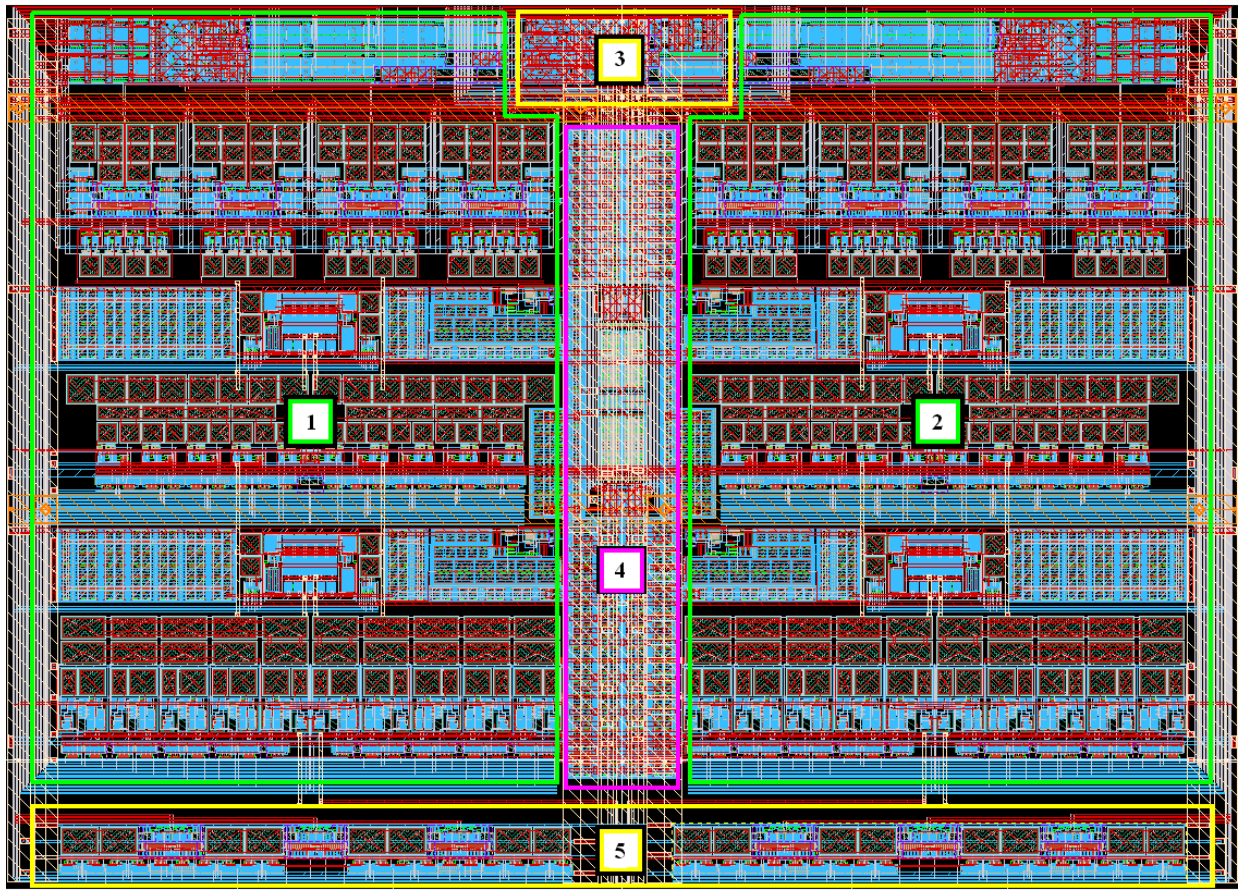

Figure 2: Layout 12-bit 2-channel 0.5 to 33 MSPS delta-sigma ADC

1. Delta-sigma modulator, I channel
2. Delta-sigma modulator, Q channel
3. Clock splitter and frequency divider
4. Bias currents
5. Input signal level detector

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology iHP SiGe BiCMOS 0.25 um
Status silicon proven
Total area 0.3 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical parameters are done for V_{cc} = 1.7÷1.9 V and T_j =-45÷+85 °C. Typical values are V_{cc} = 1.8 V and T_j= +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.7	1.8	1.9	V
Operating temperature	T_j	-	-45	27	+85	°C
Resolution	N	-	-	12	-	bit
Oversampling ratio	OSR	-	32	-	-	-
Sampling rate	F_s	-	0.5	-	33	MSPS
Bandwidth	BW	-	8	128	512	kHz
Differential peak-to-peak input voltage	$V_{in\_diff\ p\text{-}p}$	-	-	1.6	-	V
Signal-to-noise ratio	SNR	With an amplitude closed to the maximum	58	61	63	dB
Spurious free dynamic range	SFDR	-	55	63	65	dB
Common mode voltage	U	-	-	0.9	-	V
Duty cycle	S	-	45	50	55	%
Standby current	I_{st}	-	0.68	1.86	4.01	uA
Input high level voltage	V_{IH}	For digital inputs	$0.7V_{cc}$	-	V_{cc}+0.25	V
Input low level voltage	V_{IL}		-0.25	-	$0.3V_{cc}$	V

Table 2: Supply current for different input signal bands (one channel)

Input signal band	Supply current*, mA			Current register value
	min	typ.	max	
8 kHz	0.232	0.239	0.272	000001
64 kHz	0.721	0.729	0.762	000100
128 kHz	1.297	1.318	1.361	001001
256 kHz	2.365	2.483	2.512	010011
512 kHz	4.455	4.549	4.676	100111
Standby mode	0.0007	0.002	0.004	-

* - Minimal supply current corresponds to ss-corner, temperature -50 ºC; supply voltage 1.7 V;
Maximal supply current corresponds to ff-corner, temperature 85 ºC; supply voltage 1.9 V.

8 TYPICAL CHARACTERISTICS

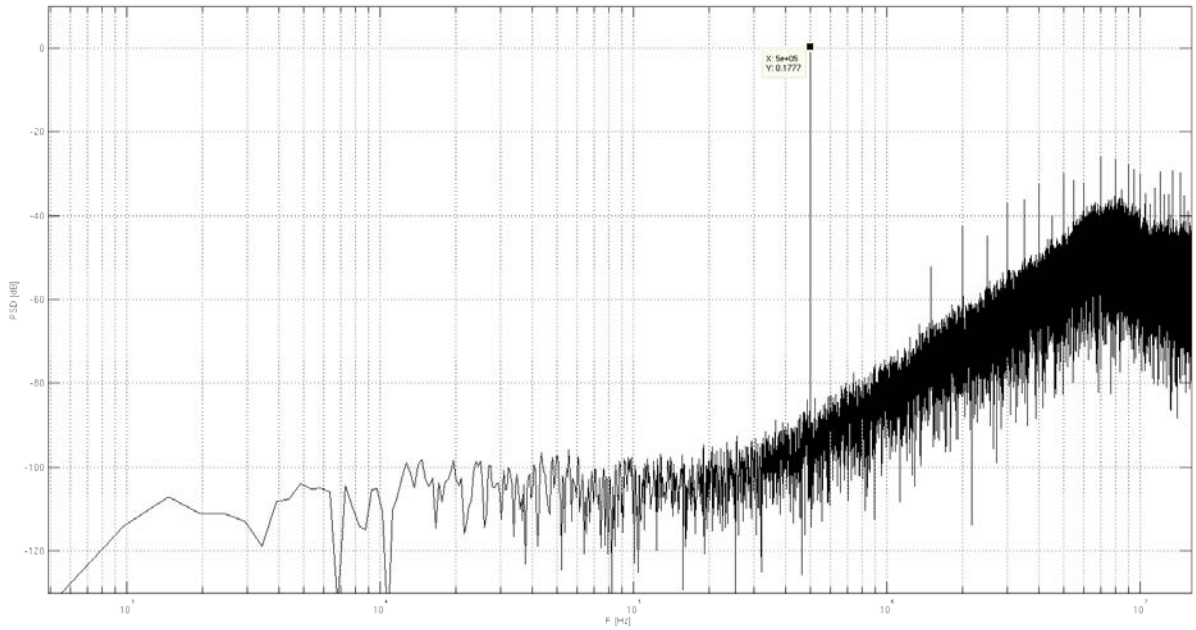

Figure 3: Output signal spectrum

Conditions:

- Fin = 500 kHz, Fclk = 32 MHz; Vin (dif p-p) = 1280 mV
- Points in calculation: 65 536
- SNR = 65.84 dB

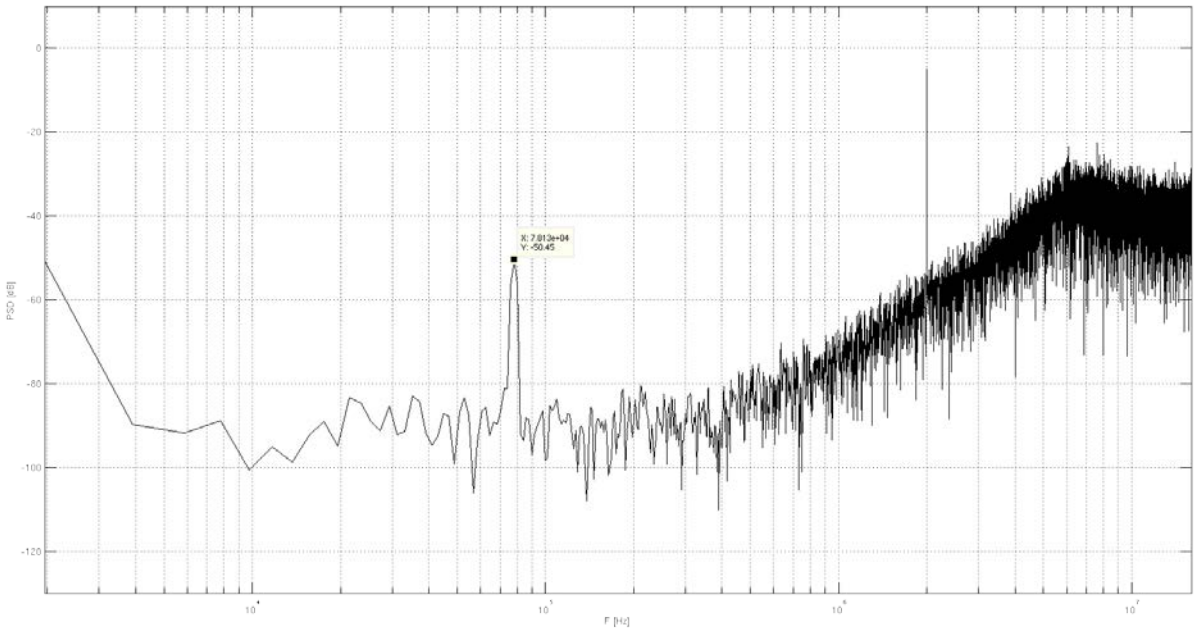

Figure 4: Output signal spectrum with the obstacle

Conditions:

- Useful signal: Fin = 78.125 kHz, Fclk = 32 MHz; Vin (dif p-p) = 4 mV
- Obstacle signal: Fin = 2 MHz, Fclk = 32 MHz; Vin (dif p-p) = 1280 mV
- Points in calculation: 16 384
- SNR = 12.59 dB

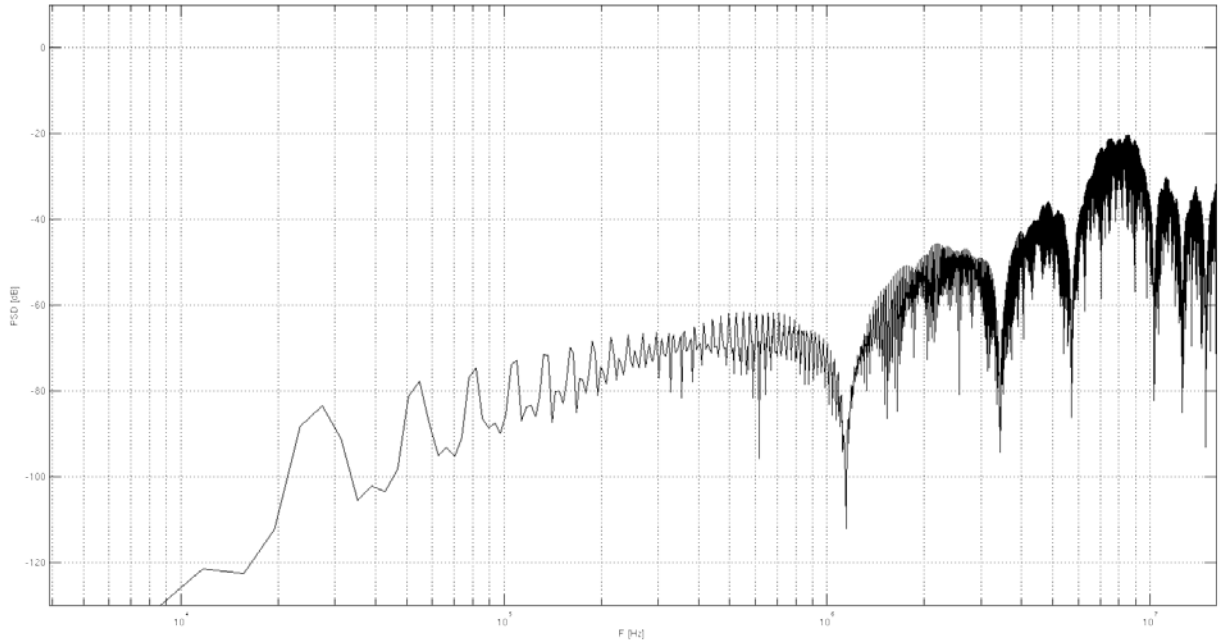

Figure 5: Output signal spectrum (common input)

Conditions:

- Fclk = 32 MHz; Vin (dif p-p) = 1280 mV
- Without tran noise
- Points in calculation: 8192

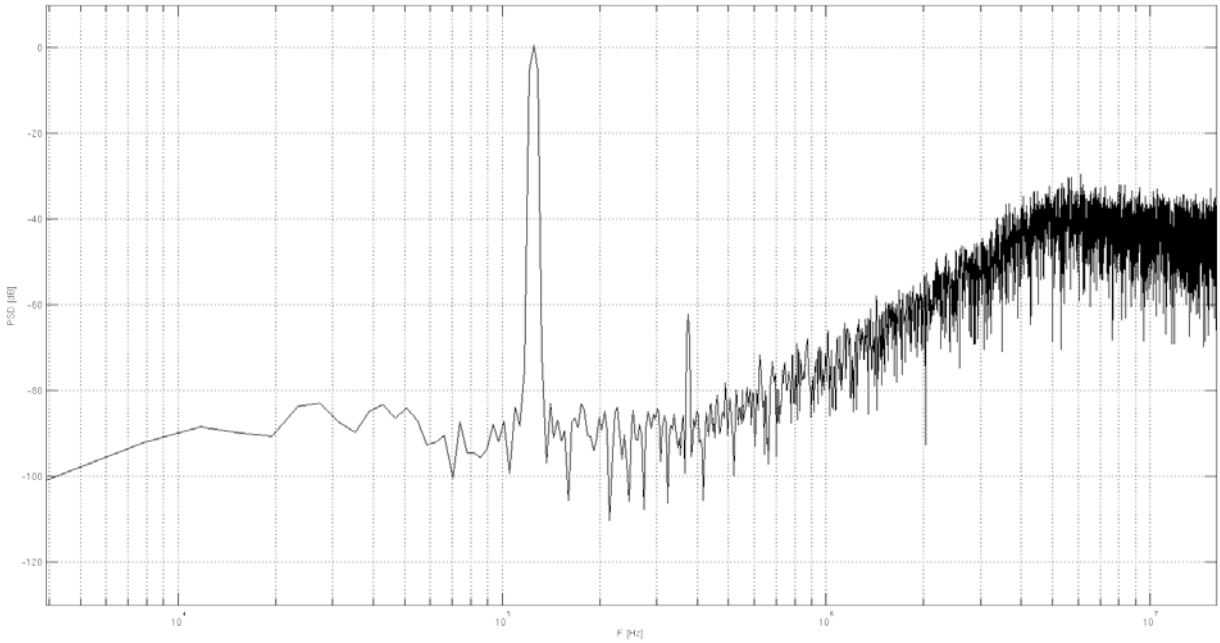

Figure 6: Output signal spectrum

Conditions:

- Fin = 128 kHz, Fclk = 32.7 MHz; Vin (dif p-p) = 320 mV
- Real reference voltages; input signal from IFA
- Points in calculation: 8192
- SNR = 58.49 dB

9 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Layout or blackbox
- Verilog, lef and lib files
- Extracted view (optional)
- HDL-description of digital filters
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.2:

- Section 4 updated

From version 1.1:

- Section 1 update
- Subsection 7.2 update