12-bit 8-channel 25 MSPS pipeline ADC

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Resolution 12 bit
- 8-channel
- Sampling frequency from 15 to 25 MHz
- Low power consumption in standby mode
- Low power dissipation (125 mW per channel)
- Signal-to-noise ratio (SNR) 61 dB
- Spurious free dynamic range (SFDR) 62 dB
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, AMS, SilTerra

2 APPLICATION

- Optical networking
- Test equipment
- Portable ultrasound and digital beam-forming systems
- Telecommunication systems
- Higher quality imaging in video systems

3 OVERVIEW

The low-power high-speed 12-bit ADC employs high-performance differential pipeline architecture.
The ADC consists of a sample and hold device, a core ADC and digital block. The ADC requires: 2.5 V analog supply, differential reference voltages 1.5 V and 1.0 V, common mode voltage 0.75 V and differential input clock.
The ADC supports standby mode which allows state with minimum power consumption.
There is also the ability to configure the operating modes of the ADC by using digital registers.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

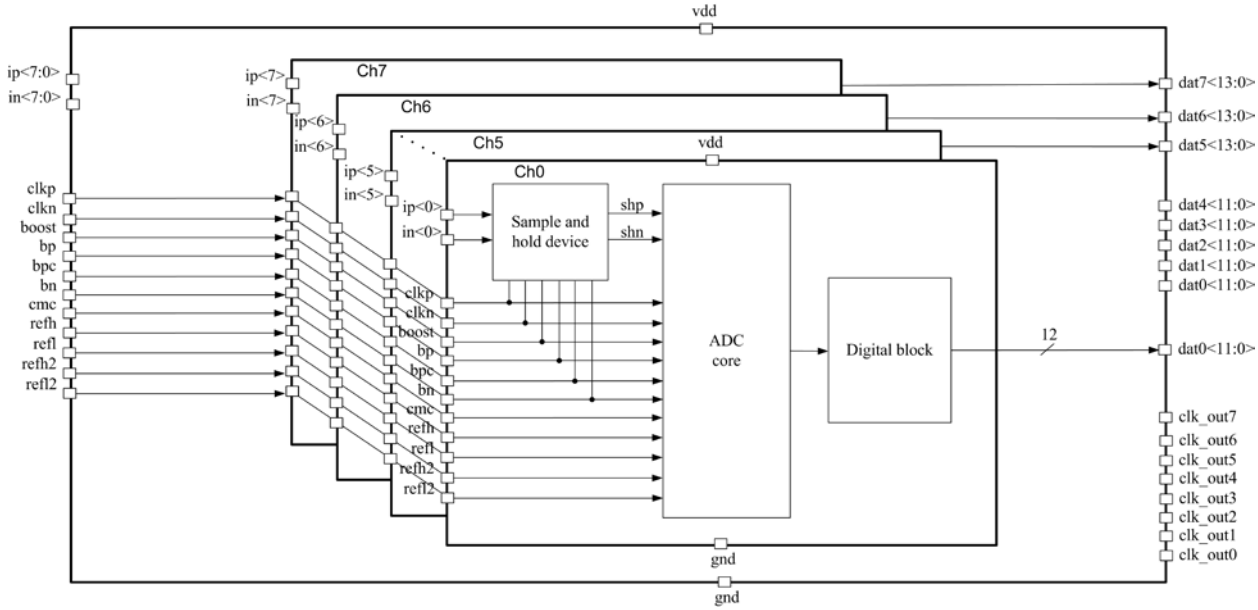

Figure 1: 12-bit 8-channel 25 MSPS pipeline ADC structure

5 PIN DESCRIPTION

Name	Direction	Description
clkp	I	Differential input clock signal
clkn		
refh	I	High level reference voltage 1.5 V
refl	I	Low level reference voltage 1 V
refh2	I	Half of the high level reference voltage
refl2	I	Half of the low level reference voltage
cmc	I	Reference level for comparators
boost	I	Reference level for keys block
bp	I	Reference level for current sources
bpc	I	Reference level for current sources
bn	I	Reference level for current sources
ip<7:0>	I	Analog differential inputs
in<7:0>		
dat0<11:0>	O	8-channels output signals
dat1<11:0>		
dat2<11:0>		
dat3<11:0>		
dat4<11:0>		
dat5<11:0>		
dat6<11:0>		
dat7<11:0>		
clk_out0<11:0>	O	8-channels output clk signals
clk_out1<11:0>		
clk_out2<11:0>		
clk_out3<11:0>		
clk_out4<11:0>		
clk_out5<11:0>		
clk_out6<11:0>		
clk_out7<11:0>		
vdd	I/O	Supply voltage 2.5 V
gnd	I/O	Ground bus

6 LAYOUT DESCRIPTION

Analog-to-digital converter layout dimensions are given in the table 1.

Table 1: Block dimensions of the 12-bit ADC

Dimension	Value	Unit
Height	2280	um
Width	2720	um

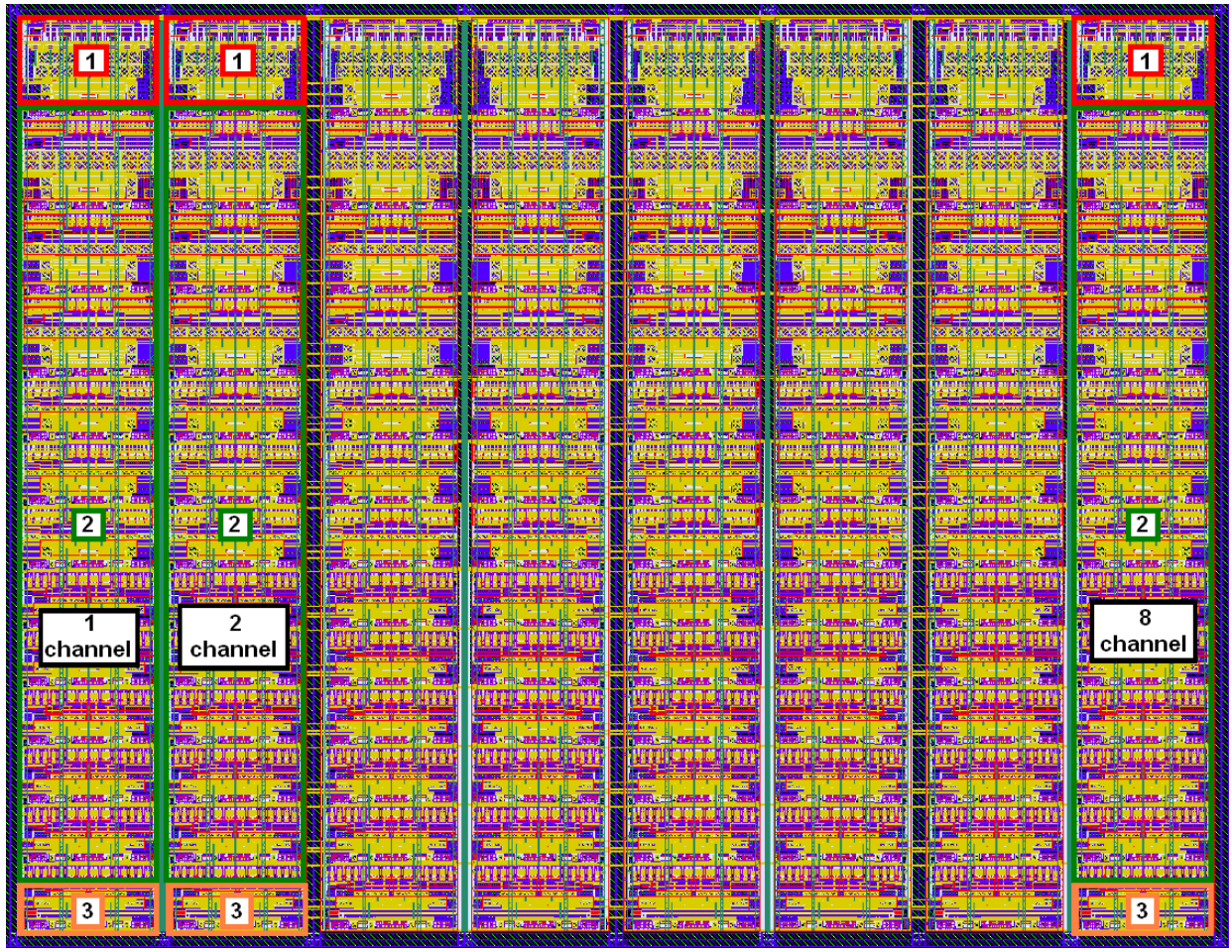

Figure 2: Layout 12-bit 8-channel 25 MSPS pipeline ADC

1. Sample and hold device
2. Block of ADC core
3. Digital block

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology iHP SiGe BiCMOS 0.25 um
Status silicon proven
Area 6.21 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd} = 2.25÷2.75 V, T_j = -60÷+125 °C. Typical values are V_{dd} = 2.5 V, T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{dd}	-	2.25	2.5	2.75	V
Operating temperature range	T_j	-	-60	+27	+125	°C
Resolution	N	-	-	12	-	bit
Maximum input amplitude	A_{IN}	-	-	0.5	-	V
Bandwidth	BW	-	7.5	10.0	12.5	MHz
Sampling rate	F_s	-	15	20	25	MSPS
Input reference voltage	V_{REF+}	-	-	1.5	-	V
	V_{REF-}		-	1	-	V
Peak-to-peak differential input voltage	$A_{IN\ p-p}$	-	-	1	-	V
DC operating point	U	-	$0.5V_{dd}$ -100mV	$0.5V_{dd}$	$0.5V_{dd}$ +100mV	V
Signal-to-noise ratio	SNR	Input amplitude $0.9A_{IN}$, input frequency 2.5 MHz, F_{clk} = 25 MHz	-	61	-	dB
Spurious free dynamic range	SFDR		56	62	64	dB
Standby current	I_{st}	-	-	60	-	uA
Current consumption	I_{dd}	For 8 channels	-	400	-	mA
Input high-logic level	V_{IH}	For digital inputs	$0.7V_{dd}$	-	V_{dd}+0.25	V
Input low-logic level	V_{IL}		-0.25	-	0.3	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.2:

- Section 3 updated
- Section 4 updated
- Section 6 updated
- Subsection 7.1 updated

From version 1.1:

- Section 1 updated
- Section 3 updated
- Subsection 7.2 updated