10-bit 2.6 kSPS ADC

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Resolution 10 bit
- Sampling rate 2.6 kSPS
- Rail-to-rail input voltage range
- 2.5 V supply voltage
- Low-power dissipation: 0.25 mW at 2.6 kSPS
- Standby mode
- Compact die area 0.04 mm^2

2 APPLICATION

- On chip temperature measurement
- On chip voltage measurement

3 OVERVIEW

IP 250iHP_ADC_09 is 10-bit 2.6 kSPS ADC employs high-performance single ended successive approximation architecture with embedded 8-input signal multiplexer. The ADC operates with sampling rate 2.6 kSPS and corresponding input clock 32 kHz. The ADC supports standby mode and features low power consumption, compact area.

4 STRUCTURE

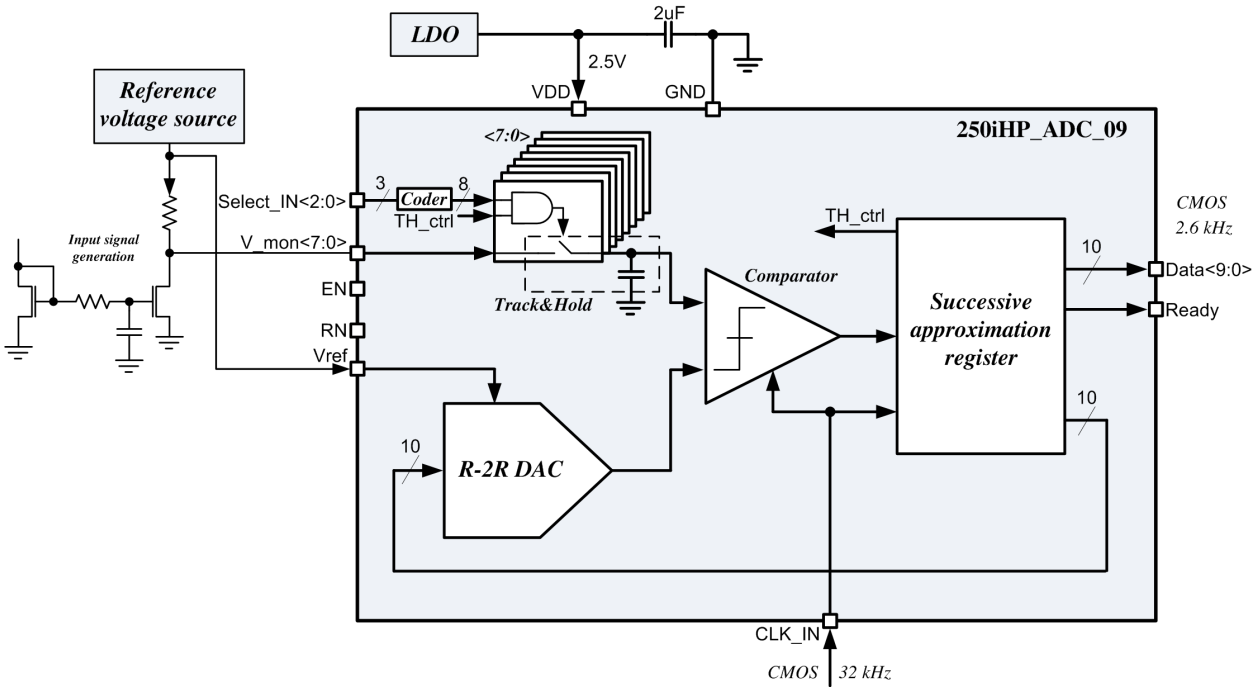

Figure 1: 10-bit 2.6 kSPS ADC application diagram

5 PIN DESCRIPTION

Name	Direction	Description	
V_mon<7:0>	I	Analog voltage input (1-of-8 input lines)	
Select_IN<2:0>	I	Input voltage line selection:	
		“000”	V_mon<0>
		“001”	V_mon<1>
		“010”	V_mon<2>
		“011”	V_mon<3>
		“100”	V_mon<4>
		“101”	V_mon<5>
		“110”	V_mon<6>
		“111”	V_mon<7>
CLK_IN	I	Clock input (32 kHz typical)	
EN	I	Block enable/disable:	
		“0”	disabled: ADC stopped, output data is holding in output register
		“1”	enabled: ADC is continuously digitizing
RN	I	Asynchronous reset:	
		“0”	reset: all registers are reset
		“1”	normal operation
Data<9:0>	O	Output data	
Ready	O	Output data ready indicator:	
		“0”	previous data holding
		“1”	new data available
th_mode	I	Input signal connection mode:	
		“0”	multiplexor mode
		“1”	track&hold mode
Vref	P	Reference voltage	
VDD	P	Supply voltage 2.5 V	
GND	P	Ground node	

Note: I – input, O – output, P – power

6 FUNCTIONAL DESCRIPTION

6.1 POWER ON AND OPERATION START

After power on the registers in digital part could set in any unknown state, which can cause wrong first run digitization. Also the ready signal could achieve "1" state which could provoke system faults. To overcome this it is recommended to hold low level voltage (logic "0") at RN input during power on to reset inner registers of ADC's digital part. Then ADC could be enabled by high voltage level (logic "1") at EN input. Note, that voltage at RN input should be high level (logic "1") during normal operation. Recommended operation start scenario is shown in figure 2.

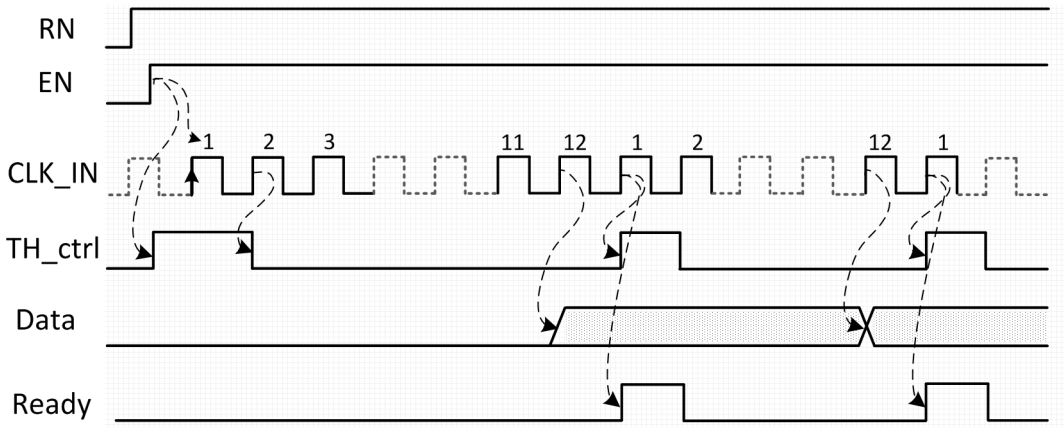

Figure 2: Power on and operation start scenario

6.2 MODES OF OPERATION

The block can operate in two modes: standby mode and active mode, which could be selected by voltage level at EN input.

- EN = "0": Standby mode. Analog blocks are disabled; inner registers excluding output data register are reset. Low power consumption
- EN = "1": Active mode. Analog blocks are enabled; digitization is carried if clock signal while clock signal is fed to CLK_IN input. There are 12 external clock cycles required to perform single digitization, so output data rate is 12 times lower than clock rate at CLK_IN input. After each digitization the Ready signal will appear with pulse width equal to external clock signal cycle (see figure 2). High power consumption

6.3 INPUT MULTIPLEXOR/TRACK&HOLD MODES AND INPUT SELECTION

1-of-8 inputs (V_mon<7:0>) could be selected for digitization by corresponding digital code at Select_IN<2:0> input.
Input switch circuit could operate in two modes according to voltage level at th_mode input:

- th_mode = "0": multiplexor mode. Only one input switch is closed, connecting corresponding V_mon input with comparator input. The other switches are opened. This mode may be used for digitizing of DC-voltage levels or very small-slope signals due to lower kick-back influence of ADC to input signal source since no switching will occur at ADC input. This mode should not be used for digitizing large signals because there will be significant voltage change at ADC input during digitization, which could cause distortion
- th_mode = "1": track&hold mode. One of the switches is closed only for sampling corresponding V_mon input voltage during one clock cycle. This voltage is stored in

capacitor at comparator input during next eleven clock cycles and is digitized by ADC. It is recommended to use ADC in this operation mode

Please note, that if voltage at inputs Select_IN<2:0> will be changed during digitization in multiplexor mode, that will cause wrong data, but if it will be changed during digitization in track&hold mode while ADC is not sampling, the output data will be correct.

6.4 OUTPUT DATA READING

Output data is available at Data<9:0> outputs of ADC. Digitization result is written to output data register at 12th clock cycle since digitization start and on the next clock cycle high voltage level (logic "1") appears at Ready output. So, output data of ADC could be grabbed by positive or negative edge of Ready signal. If voltage at EN input turns "0" some cases are possible (see figure 3):

- If voltage at EN turns "0" at the middle or beginning of digitization, than it will stop, Ready signal will remain "0", output register will hold correct previous sample data
- If voltage at EN in the end of digitization (new data is written to output register) or while Ready signal is rising up, than Ready signal will turn "1" and output register will hold correct last sample data

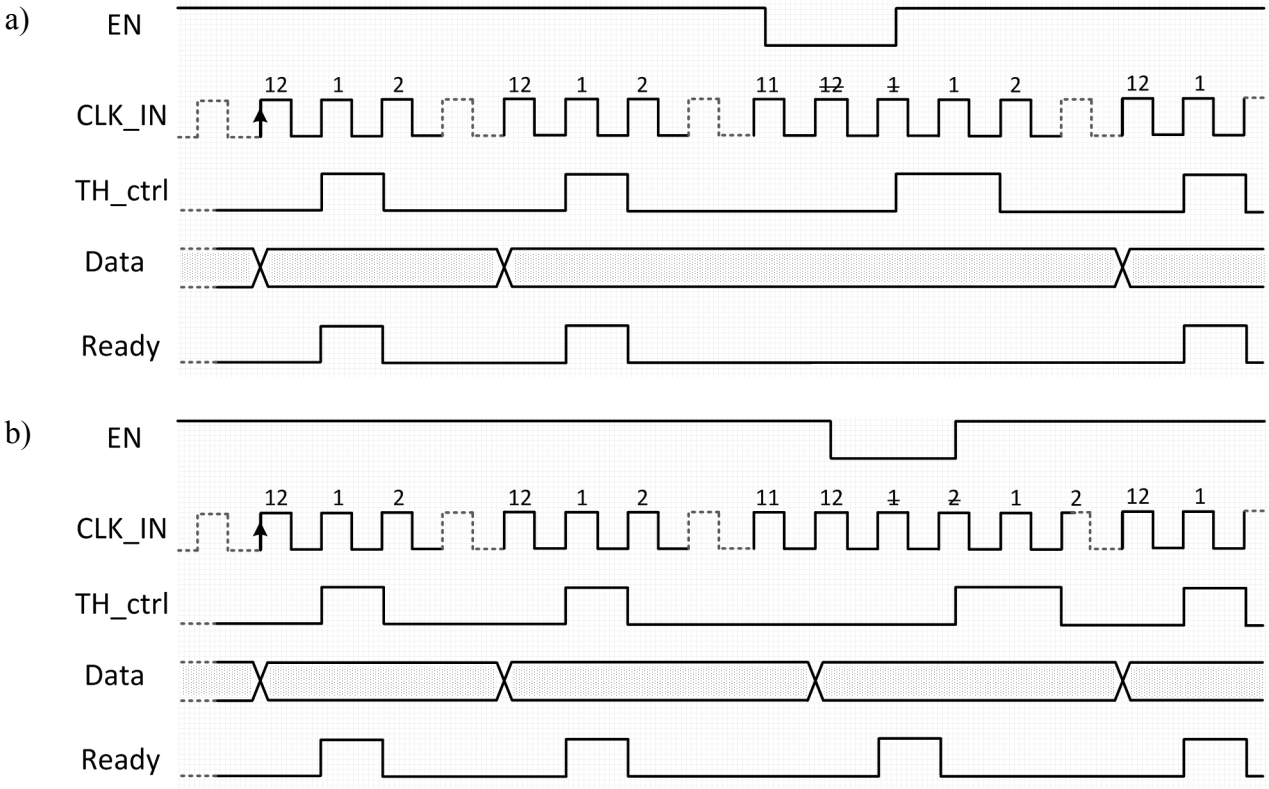

Figure 3: Data reading:
a) EN goes down during digitization; b) EN goes down after digitization and obtaining data

The ADC should not be enabled by signal at EN input after disable over less than four clock cycles. Low level voltage (logic "0") at RN input asynchronously reset all registers, including output data register and Ready. So, reading data during Reset could cause errors.

7 LAYOUT DESCRIPTION

7.1 TECHNOLOGY OPTIONS

ADC is designed under iHP 250 nm sg25H4 technology process with following options:

- 3 levels of thin metals and 1 level of thick are used for routing
- 1 level of ultra-thick metal is used for dummy fill only
- Regular Vt N/P FETs
- Rhigh and Rppd resistors
- MIM-capacitors
- No bipolar devices

7.2 PHYSICAL DIMENSIONS

Table 1: Block dimensions

Dimension	Value	Unit
Height	235	um
Width	170	um

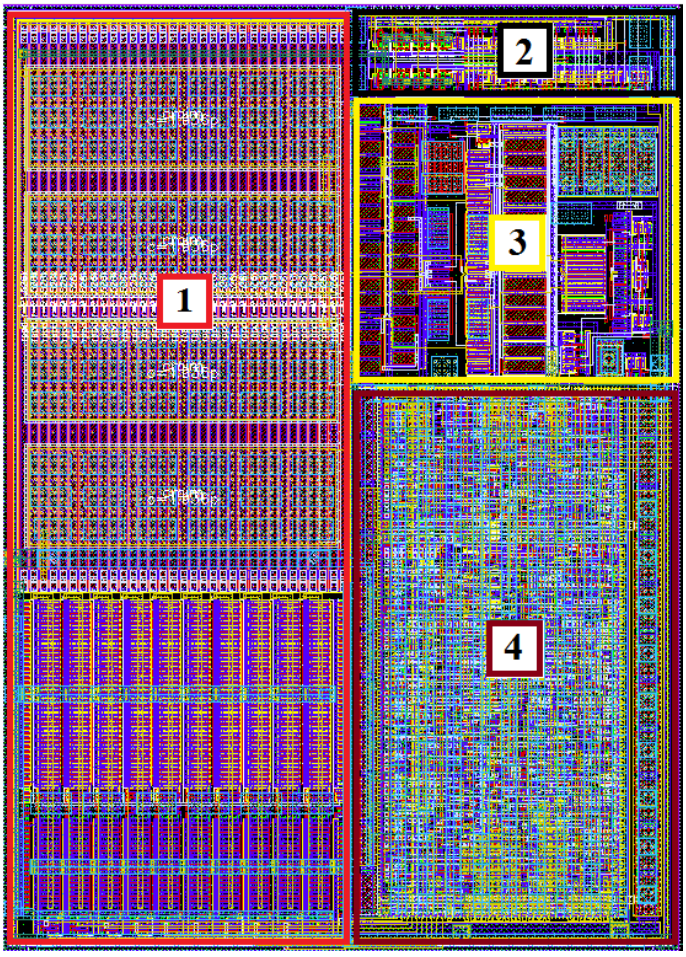

Figure 4: ADC layout

1. DAC
2. Track&Hold
3. Comparator
4. Successive approximation register

8 INTEGRATION GUIDELINES

8.1 INPUT AND OUTPUT SIGNALS

Input signals for analog-to-digital conversion should be connected to V_mon<7:0> inputs. Signal sources should be situated as close as possible to ADC inputs to minimize parasitic influence of nearby blocks and routing. During operation, the signal source is connected to ADC input capacitance of 6.5 pF through the multiplexor switch. It is recommended to feed ADC with clock frequency not lower than 12 kHz because of capacitor charge leakage.
Clock signal should be connected to input CLK_IN, which has intrinsic capacitance of 100 fF. It must have rising/falling edge no more than 2 ns. Transitions are measured at levels 0.1*VDD and 0.9*VDD (see figure 5)

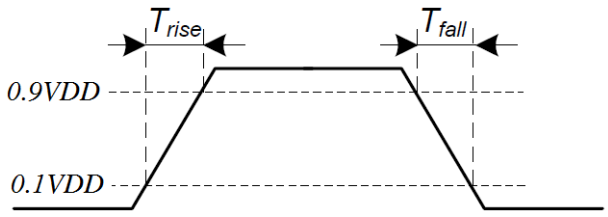

Figure 5: Input signals timing

Control inputs (Select_IN<2:0>, RN, EN, th_mode) have intrinsic capacitance of 10 fF. They must have rising/falling edge no more than 5 ns. It is supposed that these inputs will be used only for operation mode selection and normally will be unchanged during digitization. The ADC should not be enabled by signal at EN input after disable over less than four clock cycles.
Output signals (Data<9:0> and Ready) are outputs of the cells dfc3d3 of library sg025_stdcell, provided by iHP. It is not recommended to exceed 2 pF total capacitance (including parasitic), connected to ADC outputs (Data<9:0> and Ready). Note, that increasing of load capacitance at ADC outputs will increase ADC power consumption.

8.2 PLACEMENT AND ROUTING

The following requirements of placement and routing must be satisfied during integration:

1. Power supply (pin VDD), reference voltage (pin Vref) and ground (pin GND) wires must allow flowing of 500 uA current, 1.5 mA peak current and should have resistance of less than 2 Ohm each
2. No routing is allowed over the block

ADC is an analog block, which is sensitive to power supply, ground and substrate noise. So, following items below is recommended:

3. Use separate 2.5 V power supply and ground for ADC (if possible). Do not connect it to precise low noise analog blocks or to digital supplies
4. Do not place highly switching and noise circuits close to the block. Recommended space is 5-15 um and more with placed capacitance between VDD and GND in this area. Place a capacitance between VDD and GND around the block. We also recommend to place external capacitor between VDD and GND of 2 uF at least
5. Vref is separate power supply pin for internal R-2R DAC. It should also be well filtered by placing at least 20 pF capacitance between Vref and GND. Vref could also be shorted to VDD to maximize ADC scale and share filtering capacitance between these two wires

8.3 LAYOUT VERIFICATION

- DRC and LVS are run using Cadence Assura
- No dummy structures are required

9 OPERATING CHARACTERISTICS

9.1 TECHNICAL CHARACTERISTICS

Technology iHP SiGe BiCMOS 0.25 um
Status pre-silicon verification
Area 0.04 mm^2

9.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{DD} = 2.38 V ÷ 2.62 V, T = 0 °C ÷ +85 °C, A_{IN} = –1 dBFS, unless otherwise noted. Typical values are at V_{DD} = V_{REF} = 2.5 V, T = 27 °C

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
Junction Temperature	T_J	-	0	27	+85	°C
Supply Voltage	V_{DD}	-	2.38	2.50	2.62	V
Reference voltage	V_{REF}	-	1.5	2.5	V_{DD}	V
Current Consumption	I_{ST}	Standby mode	40	100	190	nA
	I_{DD}	Active mode	-	70	130	uA
Power Consumption	P_{TOTAL}	V_{REF} tied to V_{DD}	-	0.25	-	mW
Input Capacitance	C_{IN}	-	6.0	-	6.5	pF
Clock Frequency	F_{CLK}	-	12	32	-	kHz
Sample Rate	F_S	-	-	2.66	-	kSPS
Resolution	N	-	-	10	-	bit
Effective number of bits	ENOB	-	-	8	-	bit
Spurious Free Dynamic Range	SFDR	-	-	62	-	dB
Differential Nonlinearity	DNL	wrt 8bit LSB	-	-	1	LSB
Input voltage range	V_{MON}	-	0	-	V_{REF}	V
Clock Input Duty Cycle	S	-	45	50	55	%
Clock Signal Period Jitter	T_{JIT}	-	-	-	50	nS
Input Logic High Level	V_{IH}	Digital inputs and clock	$0.9V_{DD}$	-	V_{DD}	V
Input Logic Low Level	V_{IL}		0	-	0.3	V

10 TYPICAL OPERATING CHARACTERISTICS

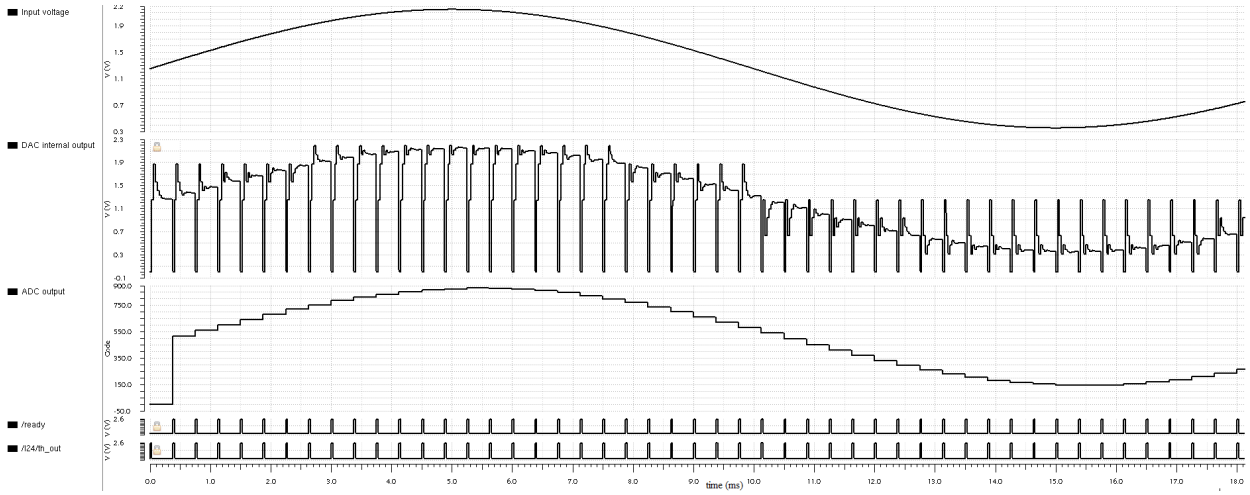

Figure 6: ADC operation flow

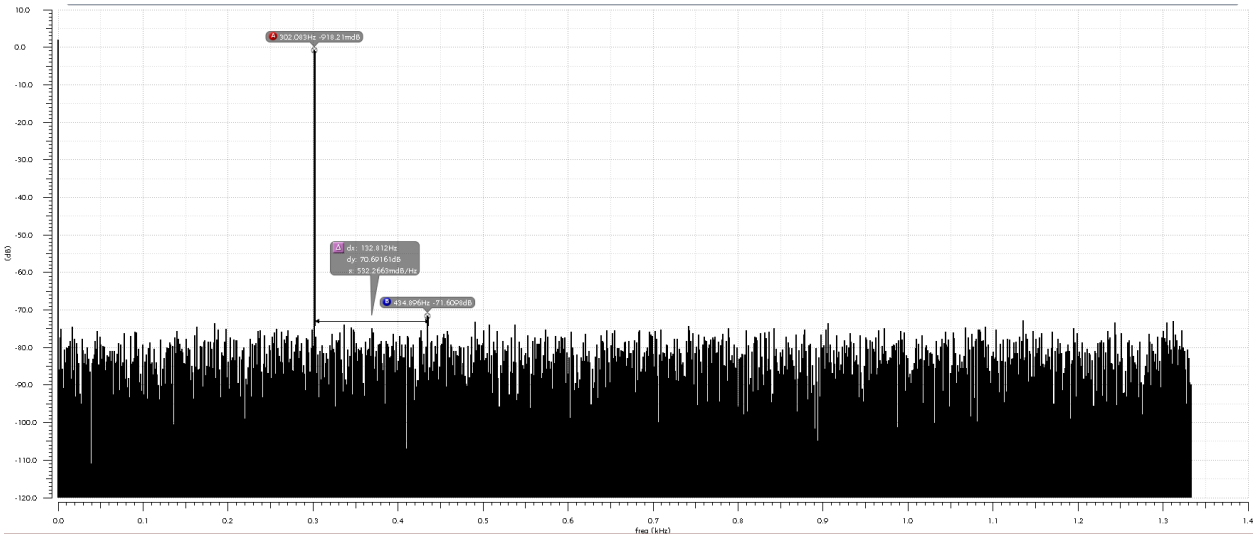

Figure 7: Output signal spectrum
Conditions: F_{IN} = 302 Hz, F_{CLK} = 32 kHz, SFDR = 70.69 dB

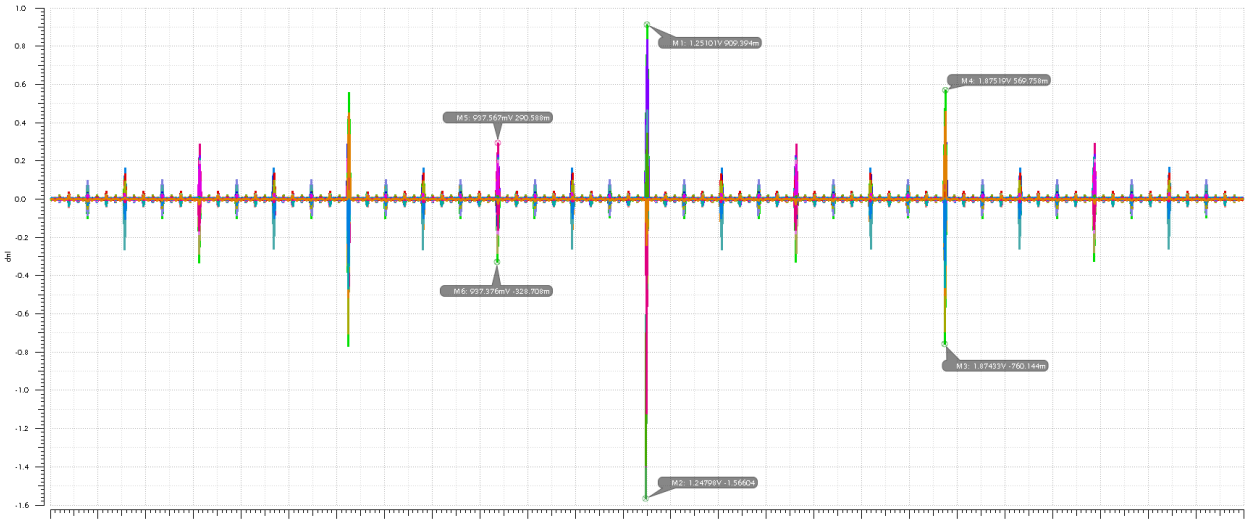

Figure 8: DNL vs Code measurement of internal DAC (Monte Carlo simulation)

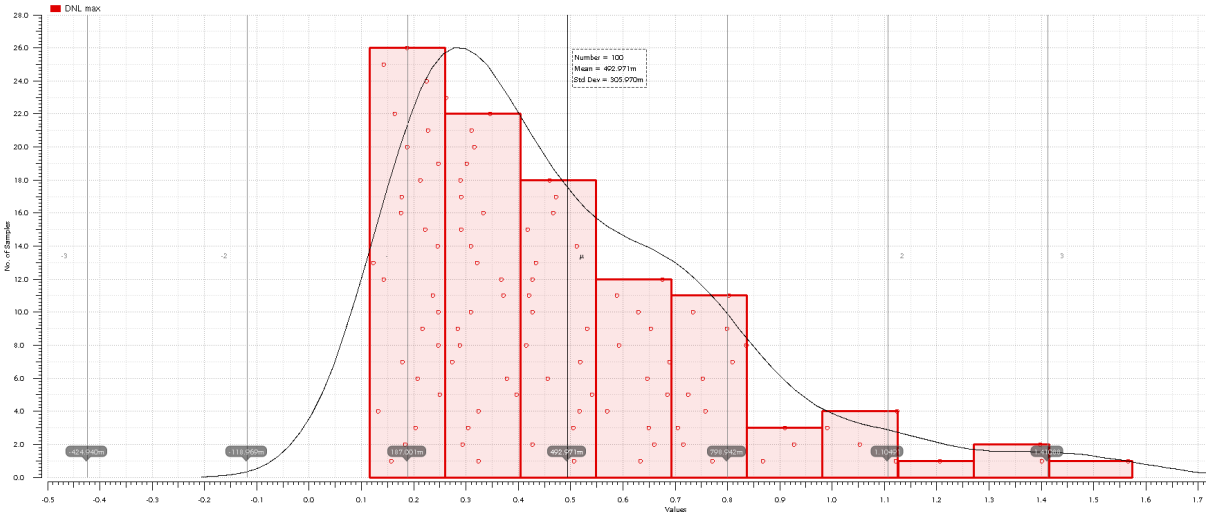

Figure 9: Absolute maximum DNL vs Code measurement of internal DAC (Monte Carlo Simulation)

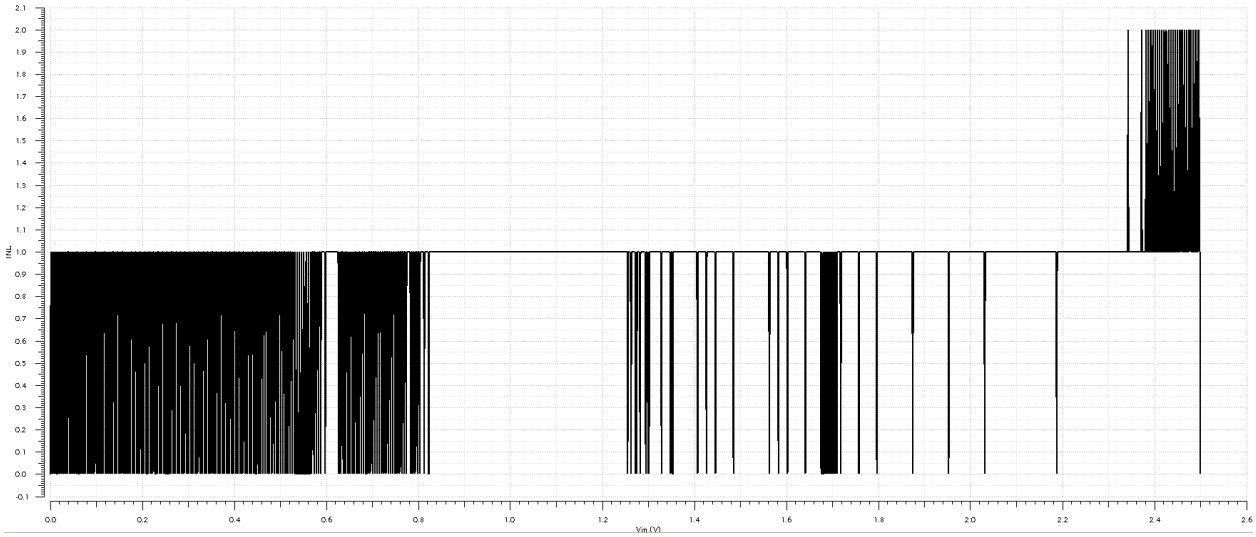

Figure 10: Integral non-linearity (INL) measurements

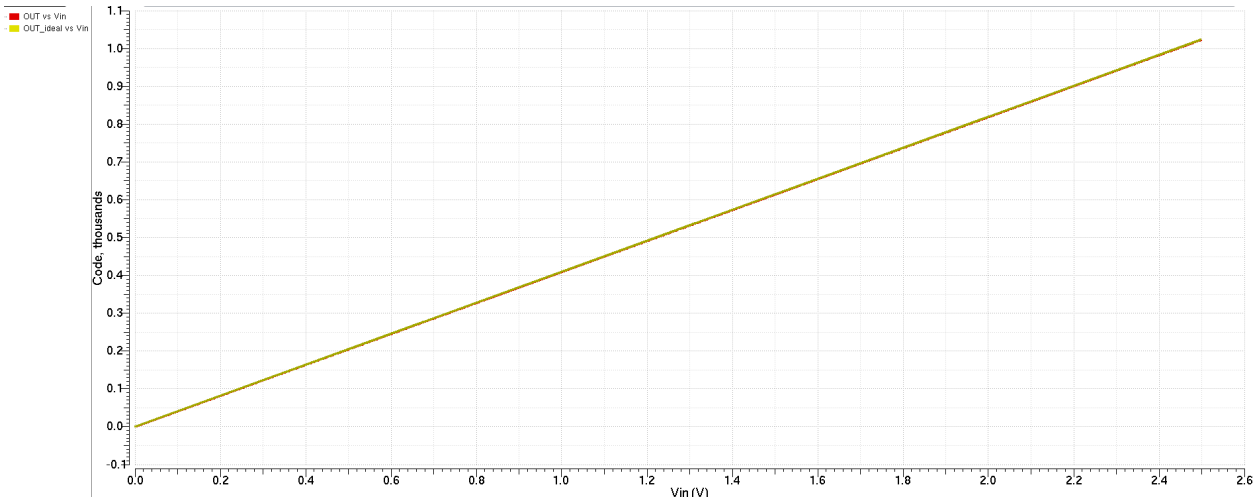

Figure 11: ADC transfer function together vs ideal ADC transfer function

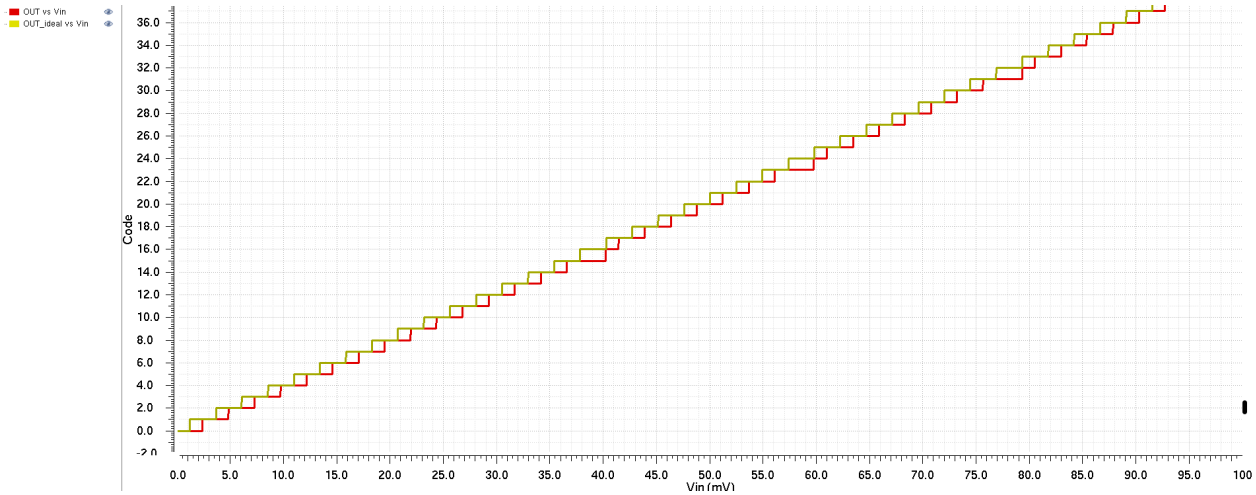

Figure 12: Low-edge ADC transfer function together vs ideal ADC transfer function

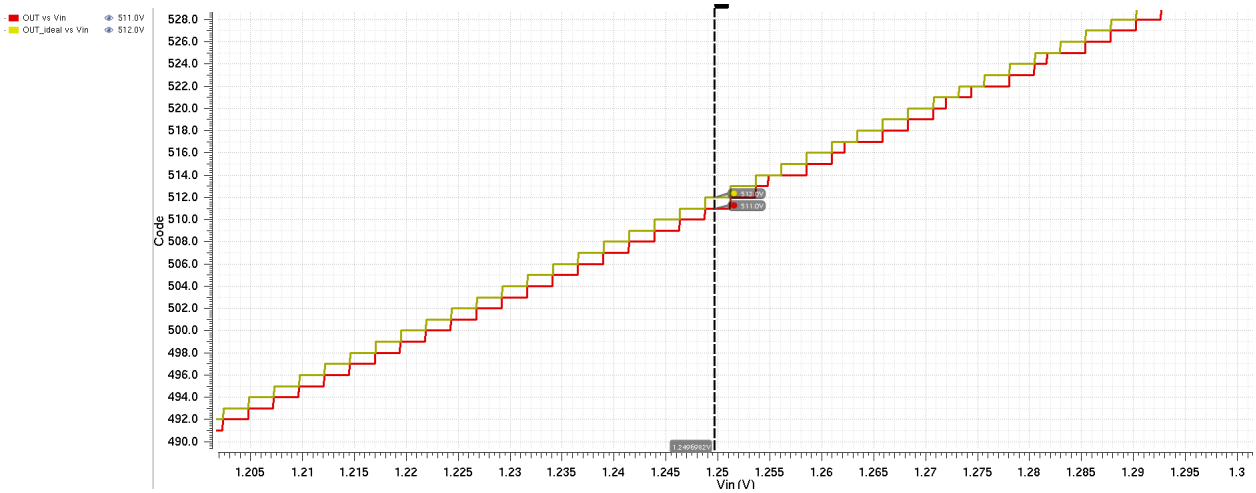

Figure 13: Middle-part ADC transfer function together vs ideal ADC transfer function

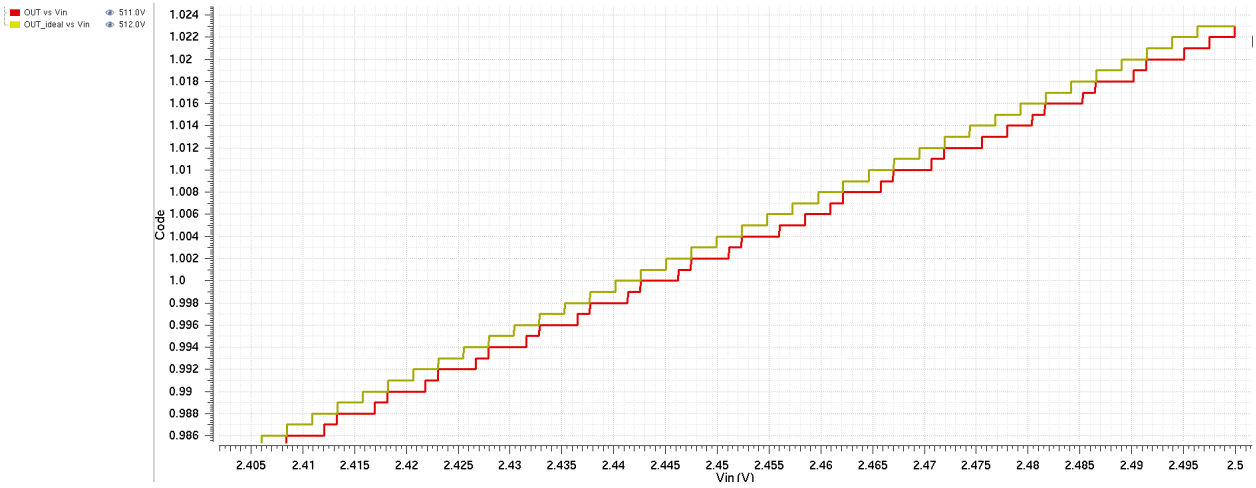

Figure 14: High-edge ADC transfer function together vs ideal ADC transfer function

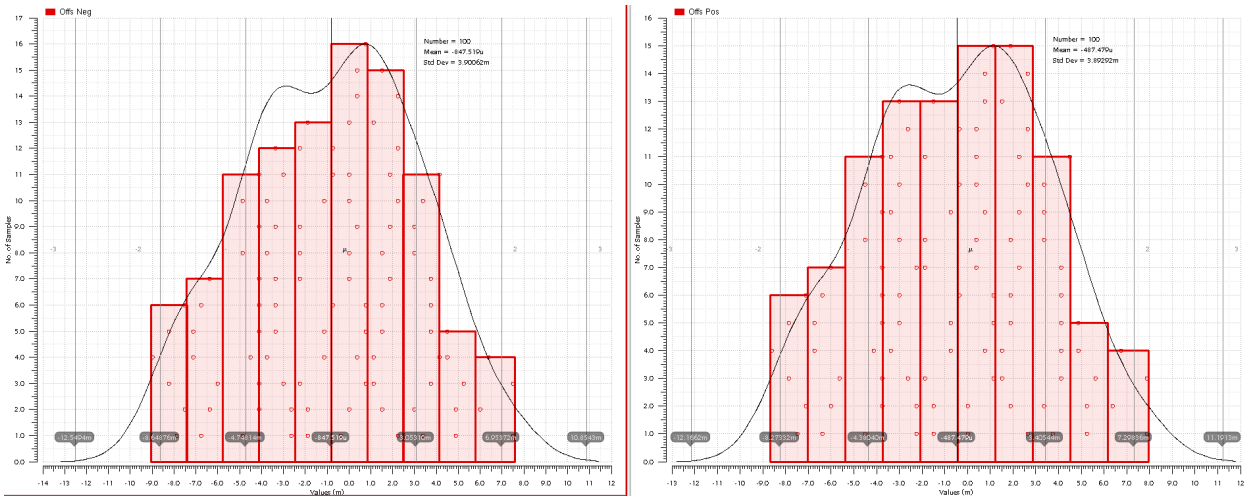

Figure 15: Comparator offset measured through Monte Carlo simulations. Sigma = 3.9mV

ADC transfer function is shown in figures 11-14. It could be seen that gain error is very low: transfer functions of designed ADC and ideal ADC differ from each other at the high-edge of transfer function for 2LSB. Then gain error could be calculated:

$$Gain\ error = Error\ in\ LSB \times \frac{FullScale}{2^{BITS}} = 2 \times \frac{2.5}{1024} = 4.9\ mV$$

For designed ADC architecture offset error mainly depends on comparator offset. For typical case with no offset in comparator the offset error at the middle code is 1LSB (see figure 13). According to possible comparator offset, obtained by Monte Carlo simulations (see figure 15), the comparator offset sigma is 3.9mV (1.6LSB for 2.5V full scale).

11 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Layout or blackbox
- Verilog, lef and lib files
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

12 THIRD PARTY IPS

250iHP_ADC_09 utilizes instances from standard logic cell library “sg025_stdcell” provided by iHP.