2-bit 50 MSPS ADC with programmable threshold

SPECIFICATION

1 FEATURES

- AMS BiCMOS 350 nm
- ADC with programmable threshold (8 thresholds)
- Resolution 2 bit
- Using voltage supply 3 V for digital and 3 V for analog parts of ADC
- Offset compensation
- Power digital buffer for PAD-work
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, SilTerra

2 APPLICATION

- Correlators
- Special processors in navigation systems
- AGS systems

3 OVERVIEW

The circuit is 2-bit ADC with programmable threshold. Logic “1” at sign output indicates, that input signal has positive polarity, “0” – indicates, that input signal has negative polarity. Similarly, the logic “1” at magn output indicates, that threshold magnitude exceeded. The threshold value is defined by external 3-bit binary code in range from 48 mV to 97 mV (table 1). The output data can be submitted in synchronous (ECL clock signal) or asynchronous modes. The chip contains offset compensation system, which operates with output sign and magn signals.

The block consists of:

- Reference voltages and currents source
- 3 asynchronous comparators which represent the core of ADC
- Offset compensation system
- Clocking signal system
- Logical “1” level convertor from 1.8 V to 3 V

Table 1: Thresholds description

Number of threshold	Binary code of threshold	Threshold value, mV
1	“000”	48
2	“001”	55
3	“010”	62
4	“011”	69
5	“100”	76
6	“101”	83
7	“110”	90
8	“111”	97

4 STRUCTURE

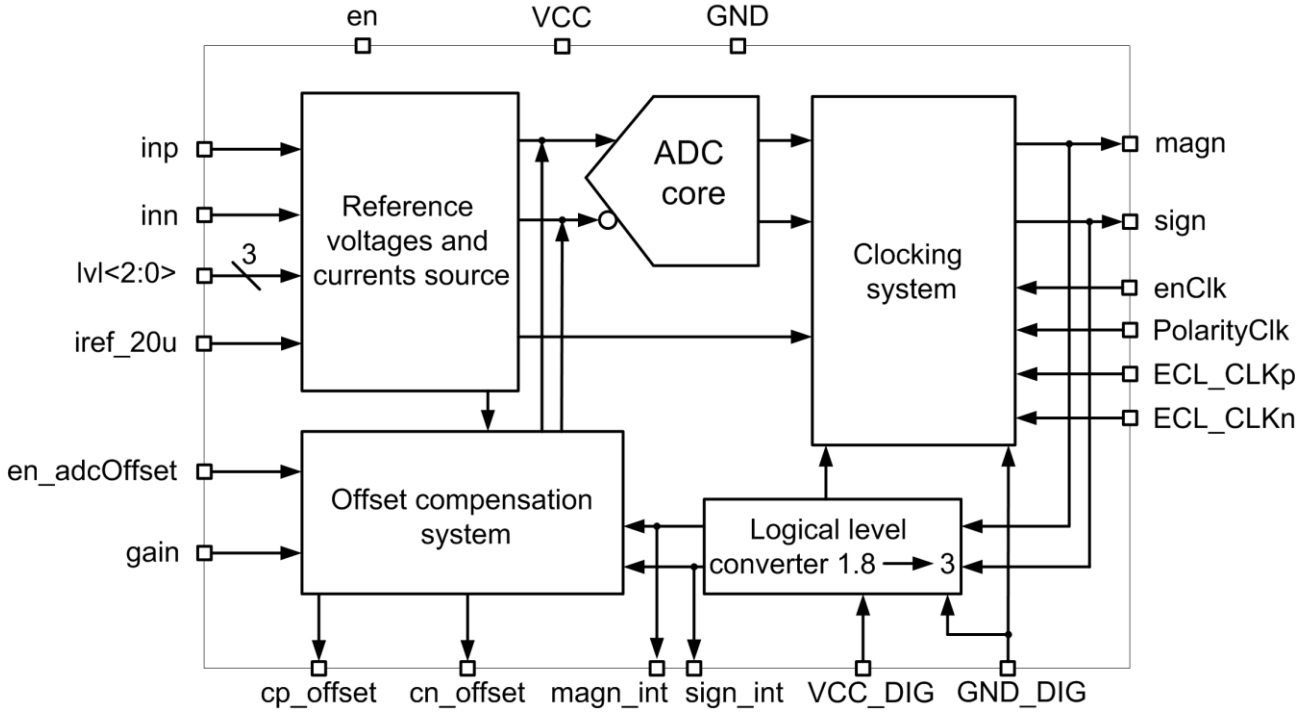

Figure 1: 2-bit 50 MSPS ADC with programmable threshold structure

5 PIN DESCRIPTION

Name	Direction	Descriptiom
iref_20u	I	Reference current 20 uA (influent)
ECL_CLKp ECL_CLKn	I	Input differential ECL-clock signal
inp inn	I	Input differential analog signal
en	I	Global enable
en_adcOffset	I	Enable of offset compensation system.
enClk	I	Enabling of clocking mode
PolarityClk	I	Clock signal polarity switch: “0” inverse “1” direct
gain	I	Gain switch of offset compensator
lvl<2:0>	I	Register of threshold selection
magn	O	Signal of excess of threshold by input signal
sign	O	Sign signal
magn_int	O	Test signal of excess of threshold by input signal
sign_int	O	Test sign signal
cp_offset cn_offset	O	Test differential signal from output of integrating cascade of offset compensator.
VCC	IO	Analog supply voltage 3 V
GND	IO	Analog ground voltage
VCC_DIG	IO	Digital buffers supply voltage 3 V
GND_DIG	IO	Digital buffers ground voltage

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 2.

Table 2: Block dimensions

Dimension	Value	Unit
Height	290	um
Width	760	um

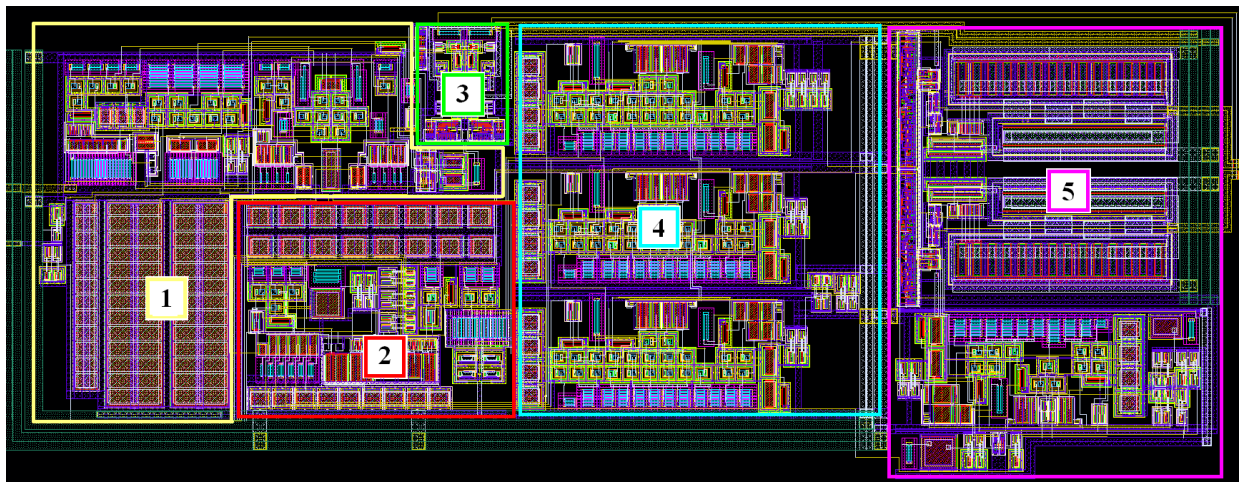

Figure 2: Layout 2-bit 50 MSPS ADC with programmable threshold

1. Offset compensation system
2. Reference voltages and currents source
3. Logical level converter 1.8 – 3.0 V
4. ADC core
5. Clocking system

7 OPERATING CHARACTERISTICS

7.1. TECHNICAL CHARACTERISTICS

Technology _____ AMS BiCMOS 0.35 um
Status _____ silicon proven
Area _____ 0.22 mm^2

7.2. ELECTRICAL CHARACTERISTICS

The values of electrical parameters are given for V_{CC} = 2.7 ÷ 3.3 V and T_j = -60 ÷ +125 °C, unless otherwise specified; typical values are given for V_{CC} = V_{CC_DIG} = 3.0 V and T_j = 27 °C.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Analog supply voltage	V_{CC}	-	2.7	3	3.3	V
Digital supply voltage	V_{CC_DIG}	-	2.7	3	3.3	V
Operating temperature	T_j	-	-60	27	+125	°C
Resolution	N	-	2	-	-	bit
Clocking frequency	F_{clk}	-	-	50	-	MHz
Sampling rate	F_S	-	-	50	-	MSPS
Bandwidth	BW	-	-	25	-	MHz
Standby power	P_{st}	-	0.13	0.19	18.81	uW
Total power	P_{supply}	Cload = 15 pF, Fin = 20 MHz, Async. mode	5.22	8.4	14.16	mW
Supply current	I_{supply}	Cload = 15 pF, Fin = 20 MHz, Async. mode	1.97	2.8	4.29	mA
Input signal common mode	U	-	-	2	-	V
Input high-logic level	V_{IH}	For digital inputs	$0.7V_{CC\_DIG}$	-	V_{CC_DIG} +0.25	V
Input low-logic level	V_{IL}		-0.25	-	$0.3V_{CC\_DIG}$	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.1:

- Section 1 updated