12-bit 500 MSPS IQ DAC

SPECIFICATION

1. FEATURES

- TSMC CMOS 65 nm
- Resolution 12 bit
- Current-sinking DAC
- Different power supplies for digital (1.2 V) and analog parts (2.5 V)
- Sampling rate up to 500 MSPS
- Optional internal differential resistive load
- Adjustable full-scale output range
- Dynamic performance:
  83.5 dB SFDR, 72.6 dB SNR at 100 MSPS and fin = 10 MHz
  77.3 dB SFDR, 73.9 dB SNR at 250 MSPS and fin = 20 MHz
  56.3 dB SFDR, 71.7 dB SNR at 500 MSPS and fin = 150 MHz
- Differential nonlinearity 0.18 LSB
- Integral nonlinearity 0.5 LSB
- Compact die area 0.47 mm^2
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2. APPLICATION

- Wireless infrastructures
- Broadband communications
- Picocell, femtocell base stations
- Medical instrumentation
- Ultrasound transducer excitation
- Signals and arbitrary waveform generators

3. OVERVIEW

The 12-bit 500 MSPS IQ DAC employs a high-performance current steering architecture and provides optional differential current output or differential voltage output. The bandgap and current source included to provide a complete DAC. The DAC can be configured to adjust full-scale output range. The DAC uses segmentation architecture combined with Q^2 random walk algorithm to achieve excellent dynamic and static performance, wide output bandwidth. An internal resistive load together with current source is used to set differential voltage output, which independent from process, supply and temperature.
The block is designed on TSMC CMOS 65 nm technology.

4. STRUCTURE

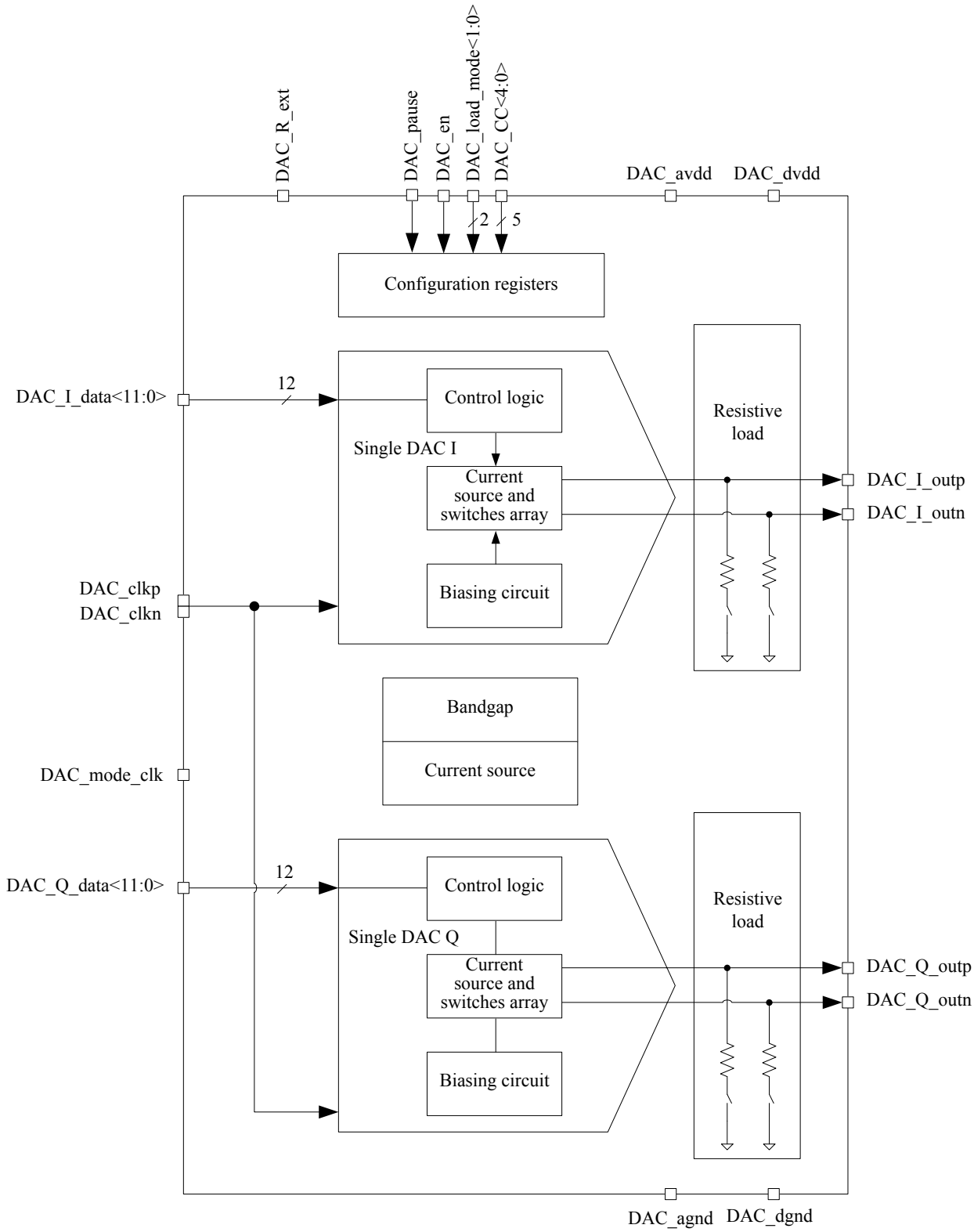

Figure 1: IQ current steering DAC module block diagram

5. PIN DESCRIPTION

Name	Direction	Description
DAC_I_data<11:0>	I	Data input of channel I
DAC_Q_data<11:0>	I	Data input of channel Q
DAC_R_ext	I	External resistor input
DAC_clkp DAC_clkn	I	500 MHz differential clock input
DAC_en	I	DAC enable: “0” disabled “1” enabled
DAC_CC<4:0>	I	Register of adjust full scale output current, if DAC_load_mode<1:0> = “0X”: “0000” 2.56 mA … ~ step 0.64 mA “1111” 22.4 mA
		Register of adjust full scale output voltage, if DAC_load_mode<1:0> = “10”: “0000” 0.128 V … ~ step 0.032 V “1111” 1.120 V
		Register of adjust full scale output voltage, if DAC_load_mode<1:0> = “11”: “0000” 0.256 V … ~ step 0.064 V “1111” 2.240 V
DAC_load_mode<1:0>	I	Load mode: “0X” an external resistive load or transformer “10” an internal differential resistive load 50 Ohm “11” an internal differential resistive load 100 Ohm
DAC_pause	I	Pause enable: “0” disabled “1” enabled
DAC_mode_clk	I	DAC input clock mode: “0” disabled ($F_{clk\ INT} = F_{clk\ EXT}$) “1” enabled ($F_{clk\ INT} = F_{clk\_EXT}/2$)
DAC_I_outp DAC_I_outn	O	Channel I differential output current
DAC_Q_outp DAC_Q_outn	O	Channel Q differential output current
DAC_avdd	P	Analog block supply voltage (2.5 V)
DAC_dvdd	P	Digital blocks supply voltage (1.2 V)
DAC_agnd	P	Analog blocks ground
DAC_dgnd	P	Digital blocks ground

6. FUNCTIONAL DESCRIPTION

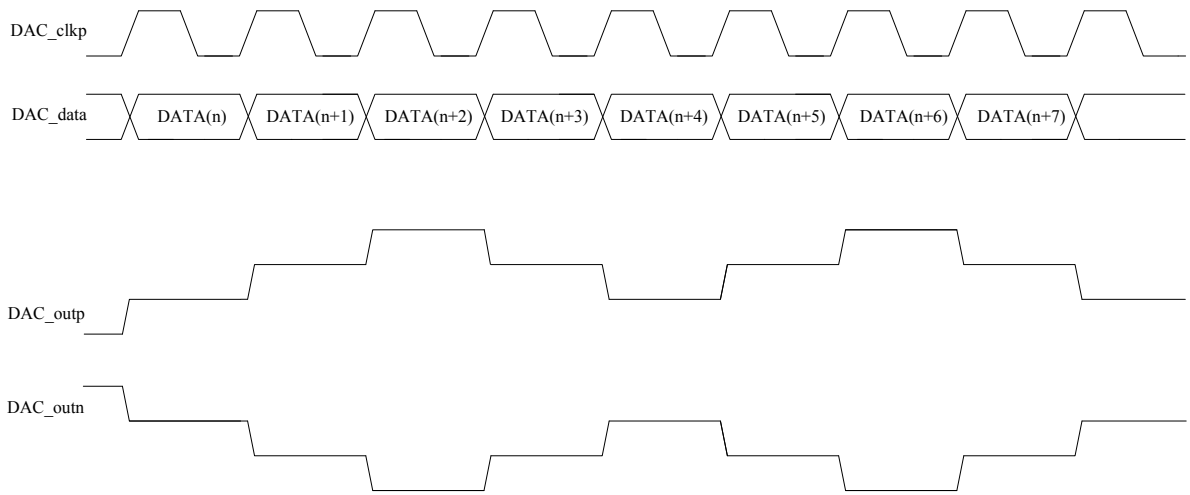

Figure 2: DAC behavior diagram

The digital input word (DAC_data) is latched on the falling edge of the clock signal (DAC_clkp). On the rising edge of the clock signal (DAC_clkp) the latched data digital word (DAC_data) is converted to its analog value at the outputs of the DAC (DAC_outp and DAC_outn).

7. FULL-SCALE OUTPUT RANGE PROGRAMMIBILITY

There is also ability to adjust full-scale output range and switch between optional internal resistive load (50 Ohm and 100 Ohm) and external resistive load.

$$A_{IOUT\ p-p} = 2.56\ mA + DAC_{CC} * 2.5uA * 256,$$

where DAC_CC – decimal representation register adjust full-scale output range.

8. LAYOUT DESCRIPTION

8.1 TECHNOLOGY OPTIONS

DAC is designed under TSMC 65 nm LP CMOS technology process with following options:

- 4x1z1u metal option
- 1.2 V standard Vt MOS
- 2.5 V MOS
- P+ polysilicon OP resistor

8.2 PHYSICAL DIMENTIONS

Dimension	Value	Unit
Height	450*	um
Width	1050*	um

*Values may be refined during the design

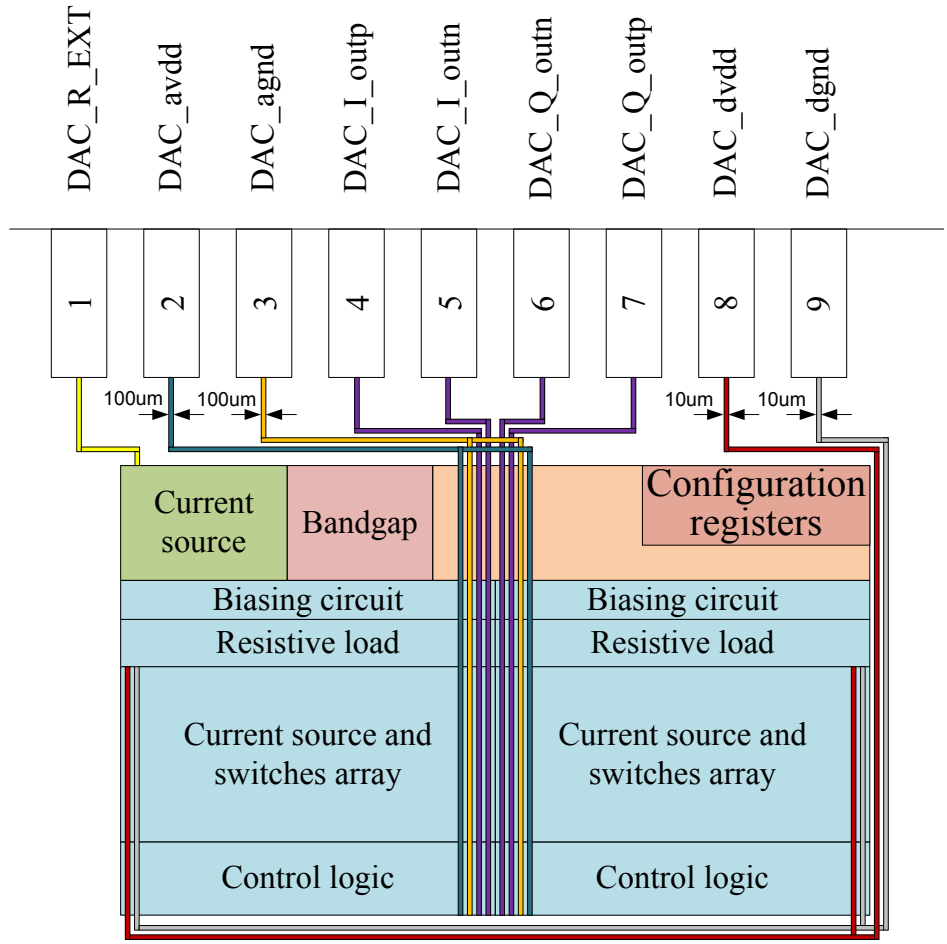

Figure 3: Layout floorplan with recommended routing

9. INTEGRATION GUIDELINES

9.1 PLACE AND ROUTE GUIDELINES

1) DAC should be place placed on a top level chip corner section or close to one edge of the top level chip.
2) DAC analog outputs DAC_I_outp, DAC_I_outn, DAC_Q_outp, DAC_Q_outn should be connected to analog IO PADs or and internal analog circuits (filter). IO PADs should not have an internal resistor to increase bandwidth.
3) DAC power supply and ground DAC_avdd, DAC_dvdd, DAC_agnd, DAC_dgnd should be connected to IO PADs.
4) Wiring of analog inputs should be symmetrical and as short as possible.
5) Noisy circuits should not place near DAC.
6) Minimum space 40 um between DAC and other circuits should be kept.
7) Minimum metal wiring width is 100 um for DAC_avdd, DAC_agnd. Multiple layers of metal can be used to reduce layout space.
8) Minimum metal wiring width is 10 um for DAC_dvdd, DAC_dgnd. Multiple layers of metal can be used to reduce layout space.
9) Allowable total resistance of DAC_avdd and DAC_agnd are 0.5 Ohm. Blocking capacitors should be added and placed as close as possible.
10) Allowable total resistance of DAC_dvdd and DAC_dgnd are 2 Ohm. Blocking capacitors should be added and placed as close as possible.

9.2 OPERATION GUIDELINES

1) Power supply decoupling should be done according the following figure. It is recommended the 100 nF capacitors to be placed as close as possible to the chip.

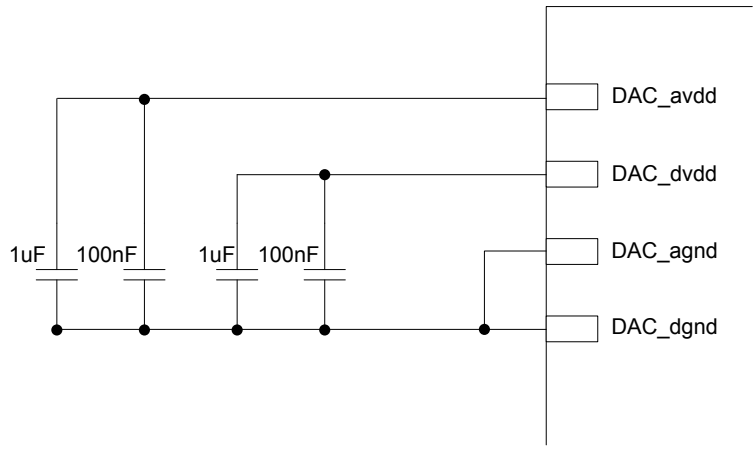

Figure 4: Power supply decoupling

10. OPERATING CHARACTERISTICS

10.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 65 nm
Status pre-silicon verification
Area 0.47 mm^2

10.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd_a} = 2.25÷2.75 V, V_{dd_d} = 1.08÷1.32 V and T_j =-40 ÷+85 °C, typical values are at V_{dd_a} = 2.5 V, V_{dd_d} = 1.2 Vand T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
Operating temperature range	T_j	-	-40	27	+85	°C
Power supply requirements						
Analog supply voltage	V_{dd_a}	-	2.25	2.5	2.75	V
Digital supply voltage	V_{dd_d}	-	1.08	1.2	1.32	V
Analog current consumption in normal mode	I_{ACN}	$A_{IOUT\ p-p}$ = 20.48 mA F_S = 500 MSPS	-	41.6	-	mA
Analog current consumption in pause mode	I_{ACP}	$A_{IOUT\ p-p}$ = 20.48 mA F_S = 500 MSPS	-	41.4	-	mA
Digital current consumption in normal mode	I_{DCN}	$A_{IOUT\ p-p}$ = 20.48 mA F_S = 500 MSPS	-	7.6	-	mA
Digital current consumption in pause mode	I_{DCP}	F_S = 500 MSPS	-	60	-	uA
Current consumption in standby mode	I_S	-	-	3	-	uA
Total power consumption in normal mode	P_{CN}	$A_{IOUT\ p-p}$ = 20.48 mA F_S = 500 MSPS P_{ACN} + P_{DCN}	-	113	-	mW
Total power consumption in pause mode	P_{CP}	$A_{IOUT\ p-p}$ = 20.48 mA F_S = 500 MSPS P_{ACP} + P_{DCP}	-	103	-	mW
DC accuracy						
Resolution	N	-	-	12	-	bit
Differential nonlinearity	DNL	-	-	0.18	-	LSB
Integral nonlinearity	INL	-	-	0.50	-	LSB
Offset error	OE	-	-	0.1	-	LSB
Gain error	GE	-	-	0.3	-	LSB
Digital inputs						
Input logic coding			Offset binary			code
Input high-logic level	V_{IH}	-	0.7 V_{dd_d}	-	-	V
Input low-logic level	V_{IL}	-	-	-	0.3 V_{dd_d}	V
Analog outputs						
Differential full-scale output current range	$A_{IOUT\ p-p}$	DAC_load_mode<1:0> = “0X” DAC_CC<4:0>=“00000”	-	2.56	-	mA
		DAC_load_mode<1:0> = “0X” DAC_CC<4:0>=“11111”	-	22.4	-	V

Table “Electrical characteristics” (continue).

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Differential full-scale output voltage range	$A_{VOUT\ p-p}$	DAC_load_mode<1:0> = “10” DAC_CC<4:0>=“00000”	-	0.256	-	V
		DAC_load_mode<1:0> = “10” DAC_CC<4:0>=“11111”	-	2.240	-	V
		DAC_load_mode<1:0> = “11” DAC_CC<4:0>=“00000”	-	0.128	-	V
		DAC_load_mode<1:0> = “11” DAC_CC<4:0>=“11111”	-	1.120	-	V
Output resistance	R_{OUT}	-	-	200	-	kOhm
Output capacitance	C_{OUT}	-	-		-	F
Output settling time	t_S	accuracy 0.1% code from 0 to FFF	-	1.2	-	ns
Output rise time	t_R	from 10% to 90%	-	130	-	ps
Output fall time	t_F	from 90% to 10%	-	110	-	ps
Digital latency	L	-				clock cycles
Timing information						
Sampling rate	F_S	-	-	-	500	MSPS
Duty cycle	S	-	45	50	55	%
Dynamic characteristic at F_S = 100 MSPS and $A_{VOUT\ p-p}$ = 1.024 V						
Signal-to-noise ratio	SNR	Fin = 10 MHz	-	72.6	-	dB
		Fin = 20 MHz	-	72.4	-	dB
		Fin = 70 MHz	-	71.8	-	dB
Spurious-free dynamic range	SFDR	Fin = 10 MHz	-	83.5	-	dB
		Fin = 20 MHz	-	68.9	-	dB
		Fin = 70 MHz	-	66.4	-	dB
Dynamic characteristic at F_S = 250 MSPS and $A_{VOUT\ p-p}$ = 1.024 V						
Signal-to-noise ratio	SNR	Fin = 10 MHz	-	73.5	-	dB
		Fin = 20 MHz	-	73.9	-	dB
		Fin = 70 MHz	-	72.5	-	dB
		Fin = 150 MHz	-	71.2	-	dB
Spurious-free dynamic range	SFDR	Fin = 10 MHz	-	81.7	-	dB
		Fin = 20 MHz	-	77.3	-	dB
		Fin = 70 MHz	-	62.4	-	dB
		Fin = 150 MHz	-	64.3	-	dB
Dynamic characteristic at F_S = 500 MSPS and $A_{VOUT\ p-p}$ = 1.024 V						
Signal-to-noise ratio	SNR	Fin = 10 MHz	-	73.1	-	dB
		Fin = 20 MHz	-	72.7	-	dB
		Fin = 70 MHz	-	74	-	dB
		Fin = 150 MHz	-	71.7	-	dB
Spurious-free dynamic range	SFDR	Fin = 10 MHz	-	81.3	-	dB
		Fin = 20 MHz	-	77.5	-	dB
		Fin = 70 MHz	-	63.4	-	dB
		Fin = 150 MHz	-	56.3	-	dB

11. TYPICAL CHARACTERISTICS

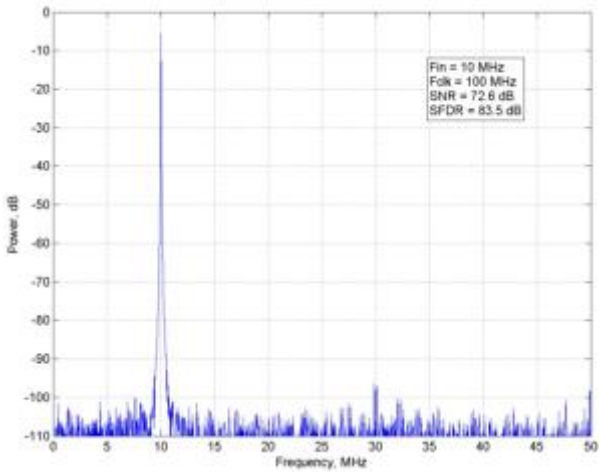

Figure 7: Spectrum with F_S = 100 MSPS, Fin = 10 MHz and $A_{VOUT\ p\text{-}p}$ = 1.024 V

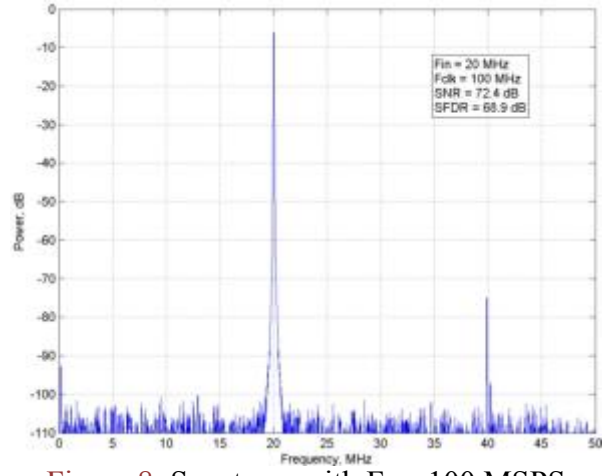

Figure 8: Spectrum with F_S = 100 MSPS, Fin = 20 MHz and $A_{VOUT\ p\text{-}p}$ = 1.024 V

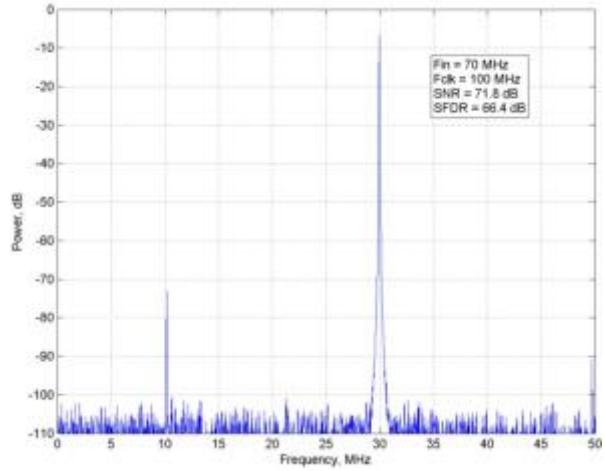

Figure 9: Spectrum with F_S = 100 MSPS, Fin = 70 MHz and $A_{VOUT\ p\text{-}p}$ = 1.024 V

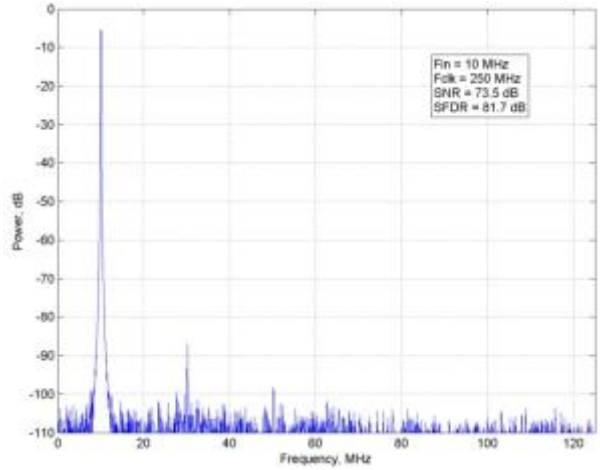

Figure 10: Spectrum with F_S = 250 MSPS, Fin = 10 MHz and $A_{VOUT\ p\text{-}p}$ = 1.024 V

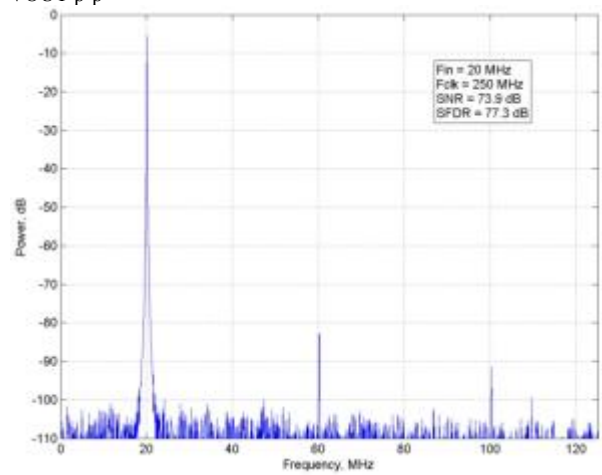

Figure 11: Spectrum with F_S = 250 MSPS, Fin = 20 MHz and $A_{VOUT\ p\text{-}p}$ = 1.024 V

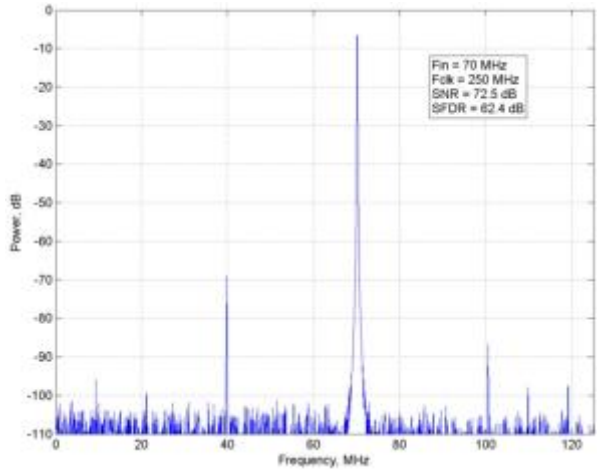

Figure 12: Spectrum with F_S = 250 MSPS, Fin = 70 MHz and $A_{VOUT\ p\text{-}p}$ = 1.024 V

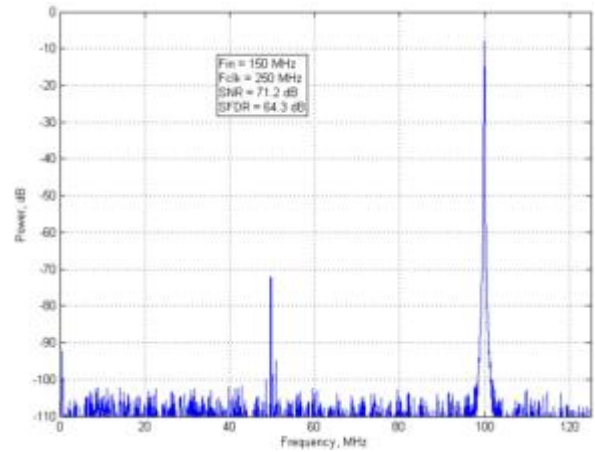

Figure 13: Spectrum with F_S = 250 MSPS, Fin = 150 MHz and $A_{VOUT\ p\text{-}p}$ = 1.024 V

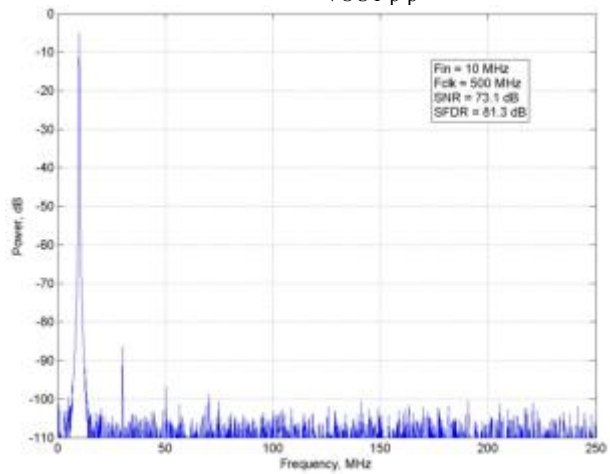

Figure 14: Spectrum with F_S = 500 MSPS, Fin = 10 MHz and $A_{VOUT\ p\text{-}p}$ = 1.024 V

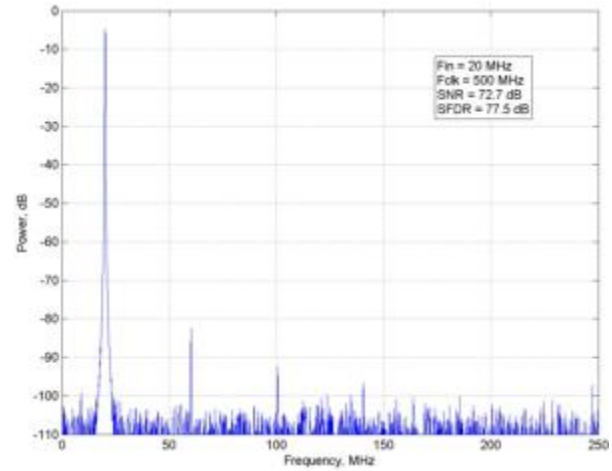

Figure 15: Spectrum with F_S = 500 MSPS, Fin = 20 MHz and $A_{VOUT\ p\text{-}p}$ = 1.024 V

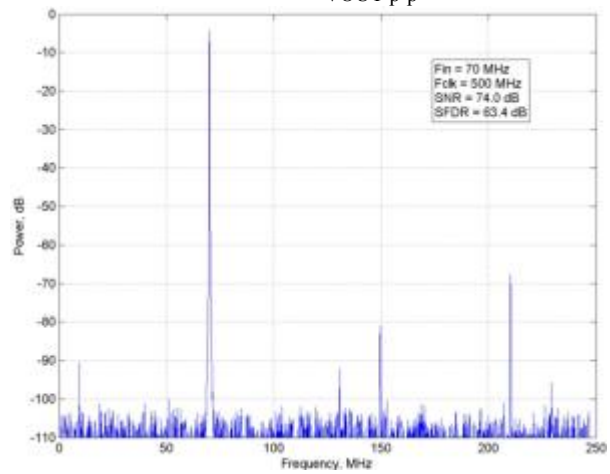

Figure 16: Spectrum with F_S = 500 MSPS, Fin = 70 MHz and $A_{VOUT\ p\text{-}p}$ = 1.024 V

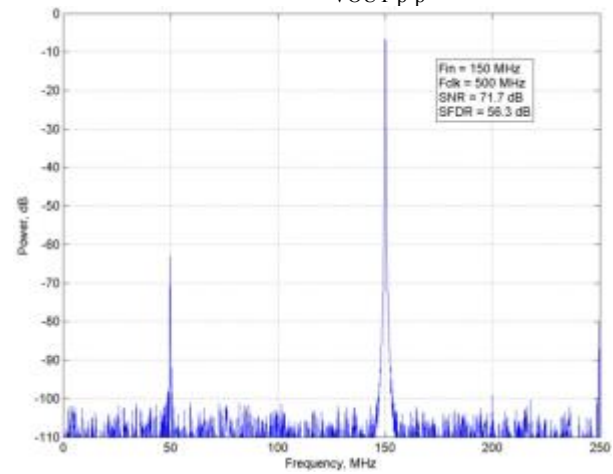

Figure 17: Spectrum with F_S = 500 MSPS, Fin = 150 MHz and $A_{VOUT\ p\text{-}p}$ = 1.024 V

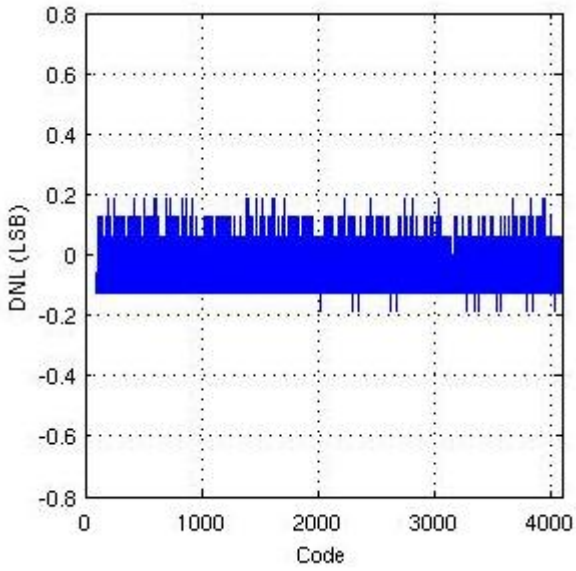

Figure 18: Differential nonlinearity

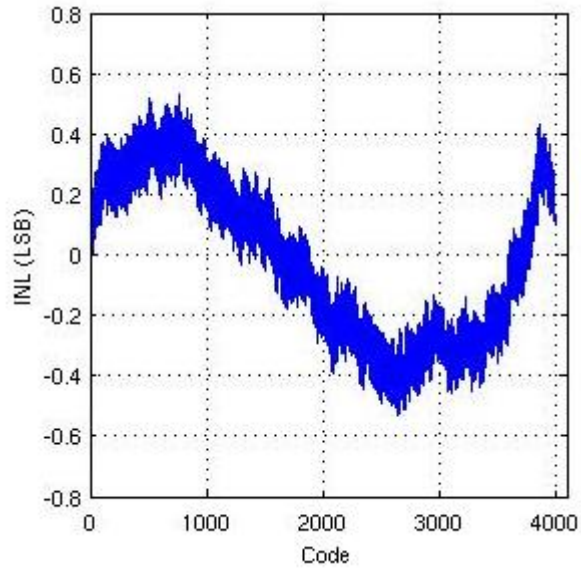

Figure 19: Integral nonlinearity

12. DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation