12-bit 140 MSPS IQ DAC

SPECIFICATION

1 FEATURES

- TSMC CMOS 65 nm
- Resolution 12 bit
- Current-sinking DAC
- Different power supplies for digital (1.2 V) and analog parts (2.5 V)
- Sampling rate up to 140 MSPS
- Optional internal differential resistive load
- Adjustable full-scale output range
- Dynamic performance:
  SFDR= 70 dB, NSD= 144.6 dBm/Hz for F_{clk} = 140 MHz and F_{in}= 5 MHz
  SFDR= 61.6 dB, NSD= 143.9 dBm/Hz for F_{clk} = 140 MHz and F_{in}= 30 MHz
- Differential nonlinearity 0.18 LSB
- Integral nonlinearity 0.5 LSB
- Compact die area 0.66 mm^2
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Wireless infrastructures
- Broadband communications
- Picocell, femtocell base stations
- Medical instrumentation
- Ultrasound transducer excitation
- Signals and arbitrary waveform generators

3 OVERVIEW

The 12-bit 140 MSPS IQ DAC employs a high-performance current steering architecture and provides optional differential current output or differential voltage output. The bandgap and current source are included to provide a complete DAC. The DAC can be configured to adjust full-scale output range. The DAC uses segmentation architecture combined with Q^2 random walk algorithm to achieve excellent dynamic and static performance, wide output bandwidth. An internal resistive load together with current source is used to set differential voltage output, which independent from process, supply and temperature. LVDS transmitter, output buffers and IO PADs are included.
The block is designed on TSMC CMOS 65 nm technology.

4 STRUCTURE

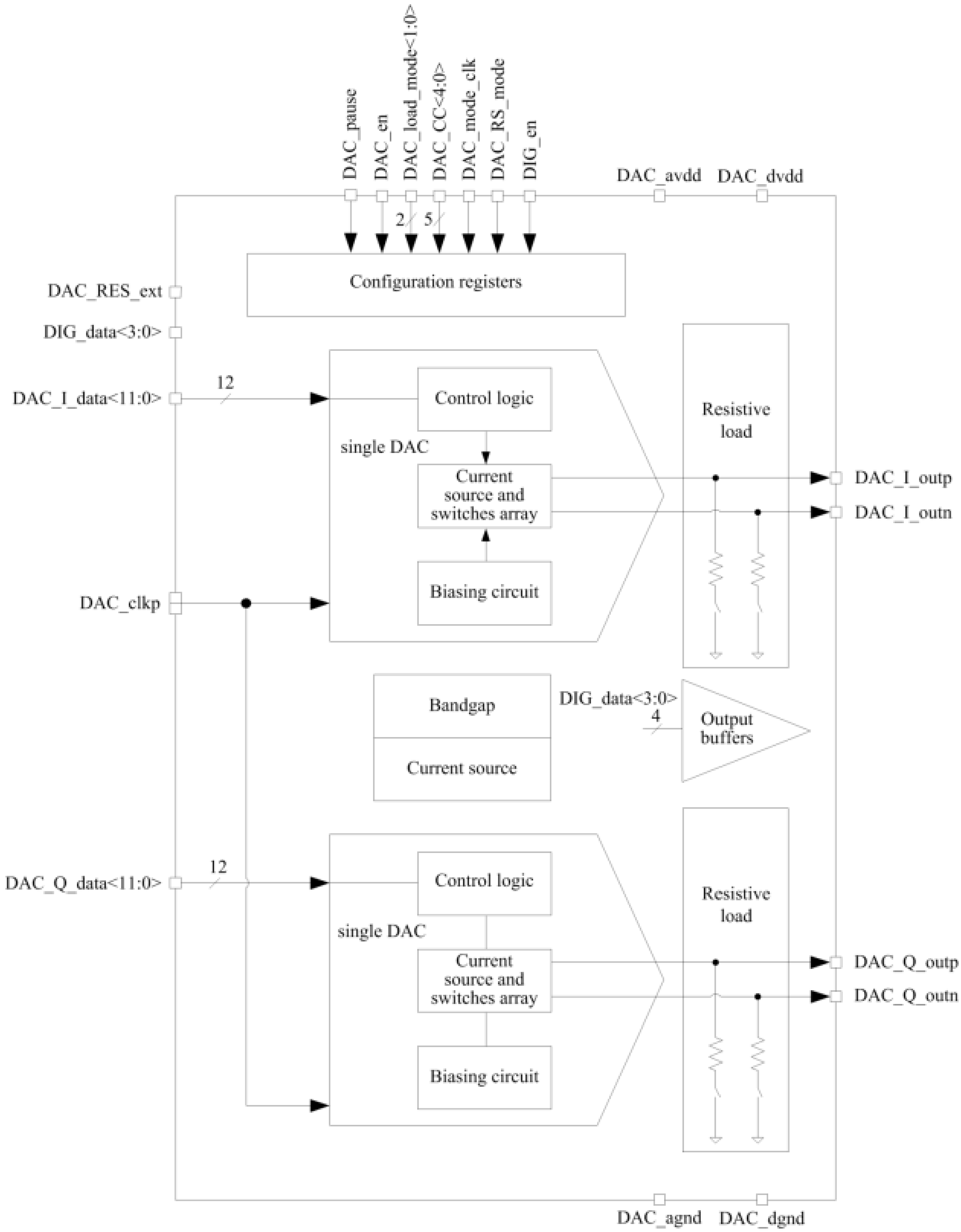

Figure 1: IQ current steering DAC module block diagram

5 PIN DESCRIPTION

Name	Direction	Description
DAC_I_outp DAC_I_outn	O	Differential output current of channel I
DAC_Q_outp DAC_Q_outn	O	Differential output current of channel Q
DAC_en	I	DAC enable: "0" disabled "1" enabled
DAC_pause	I	Pause enable: "0" disabled "1" enabled
DIG_en	I	Output buffers enable: "0" disabled "1" enabled
DAC_mode_clk	I	Divider enable: "0" disabled ($F_{clk\_INT} = F_{clk\_EXT}$) "1" enabled ($F_{clk\_INT} = F_{clk\_EXT}/2$)
DAC_I_data<11:0>	I	Data input of channel I
DAC_Q_data<11:0>	I	Data input of channel Q
DAC_RES_ext	I	External resistor input
DAC_clkp	I	140 MHz clock input
DAC_CC<4:0>	I	Register of adjust full scale output current if DAC_load_mode<1:0> = "0X": "00000" 2.56 mA … with step of 0.64 mA "11111" 22.4 mA
		Register of adjust full scale output voltage if DAC_load_mode<1:0> = "10": "00000" 0.128 V … with step of 0.032 V "11111" 1.120 V
		Register of adjust full scale output voltage if DAC_load_mode<1:0> = "11": "00000" 0.256 V … with step of 0.064 V "11111" 2.240 V
DAC_load_mode<1:0>	I	Load mode: "0X" an external resistive load or transformer "10" an internal differential resistive load 50 Ohm "11" an internal differential resistive load 100 Ohm
DAC_RS_mode	I	Resistor defining reference current mode: "0" an external resistor "1" an internal resistor
DIG_data<3:0>	I	Data input
DAC_avdd	I/O	Analog blocks supply voltage (2.5 V)
DAC_dvdd	I/O	Digital blocks supply voltage (1.2 V)
DAC_agnd	I/O	Analog blocks ground
DAC_dgnd	I/O	Digital blocks ground

6 FUNCTIONAL DESCRIPTION

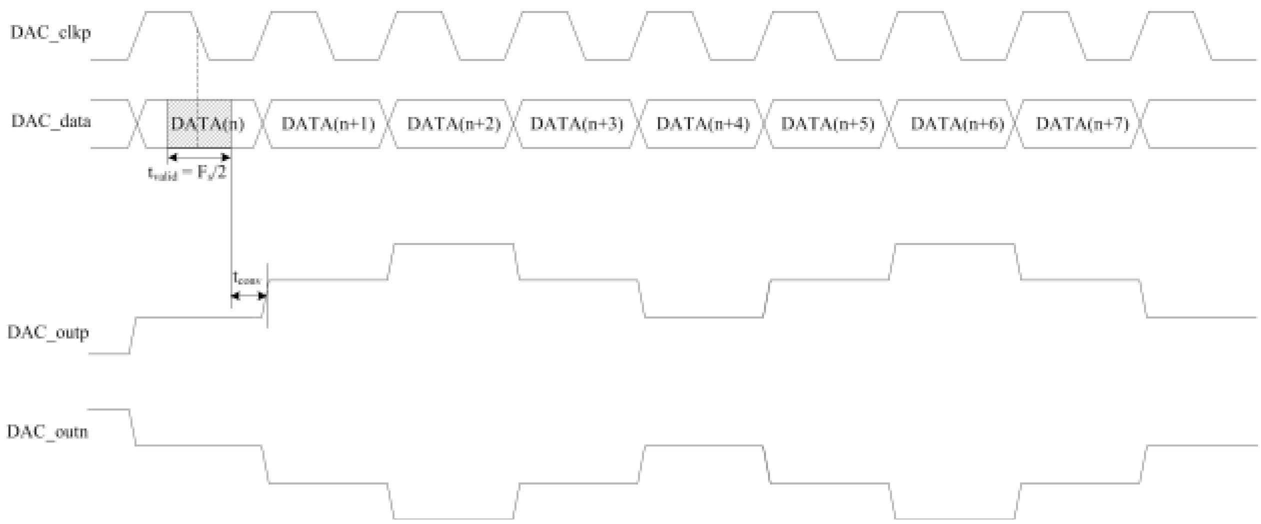

Figure 2: DAC behavior diagram

The digital input word (DAC_data) is latched on the falling edge of the clock signal (DAC_clkp). On the rising edge of the clock signal (DAC_clkp) the latched data digital word (DAC_data) is converted to its analog value at the outputs of the DAC (DAC_outp and DAC_outn).

6.1 FULL-SCALE OUTPUT RANGE PROGRAMMIBILITY

There is also ability to adjust full-scale output range and switch between optional internal resistive load (50 Ohm and 100 Ohm) and external resistive load.

$$A_{IOUT\ p-p} = 2.56\ \text{mA} + DAC_{CC} * 2.5\ \text{uA} * 256,$$

where DAC_CC – decimal representation register adjust full-scale output range.

6.2 OUTPUT BUFFER

There is also ability to use four output buffers, where first buffer has input DIG_data<0> and output DAC_I_outp, second buffer – input DIG_data<1> and output DAC_I_outn, third buffer – input DIG_data<2> and output DAC_Q_outn, fourth – input DIG_data<3> and output DAC_Q_outp. Control signals DAC_en should be set in “0”.

7 LAYOUT DESCRIPTION

7.1 TECHNOLOGY OPTIONS

DAC is designed under TSMC LP CMOS 65 nm technology process with following options:

- 4x1z1u metal option
- 1.2 V standard Vt MOS
- 2.5 V MOS
- P+polysilicon OP resistor

7.2 PHYSICAL DIMENTIONS

DAC layout dimensions are given in the table 1.

Table 1: DAC dimensions

Dimension	Value	Unit
Height	570	um
Width	1157	um

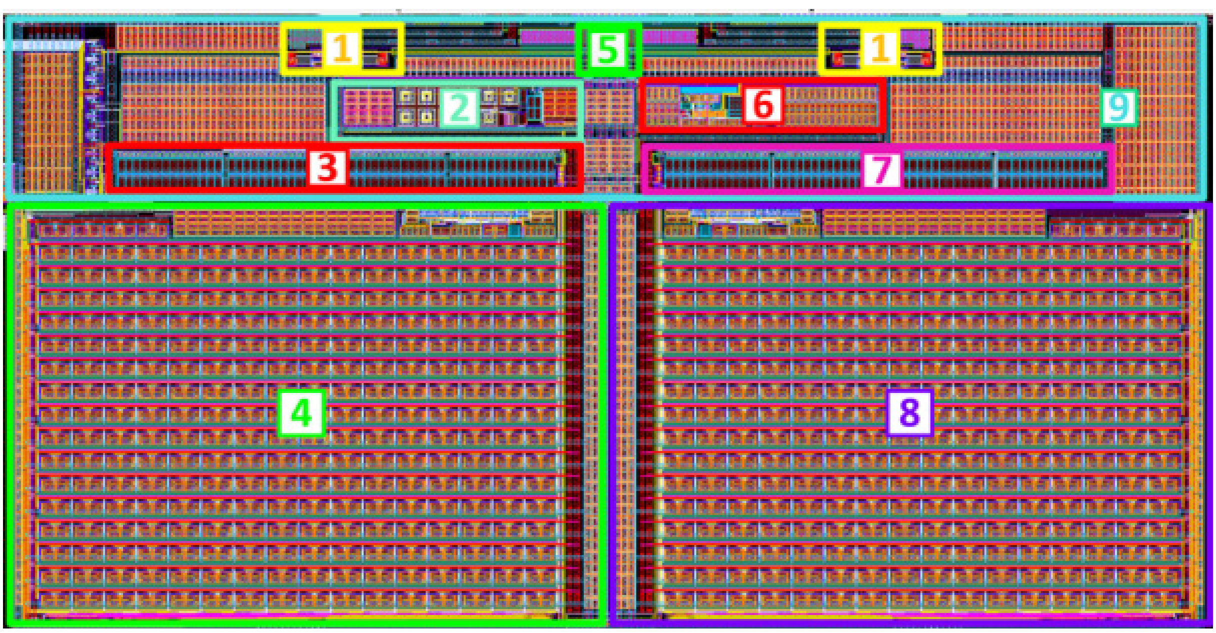

Figure 3: DAC layout

1. Output buffers
2. Bandgap
3. Resistive load I
4. DAC single I
5. Configuration registers
6. Current source
7. Resistive load Q
8. DAC single Q
9. Blocking capacitors

7.3 LAYOUT FLOORPLAN

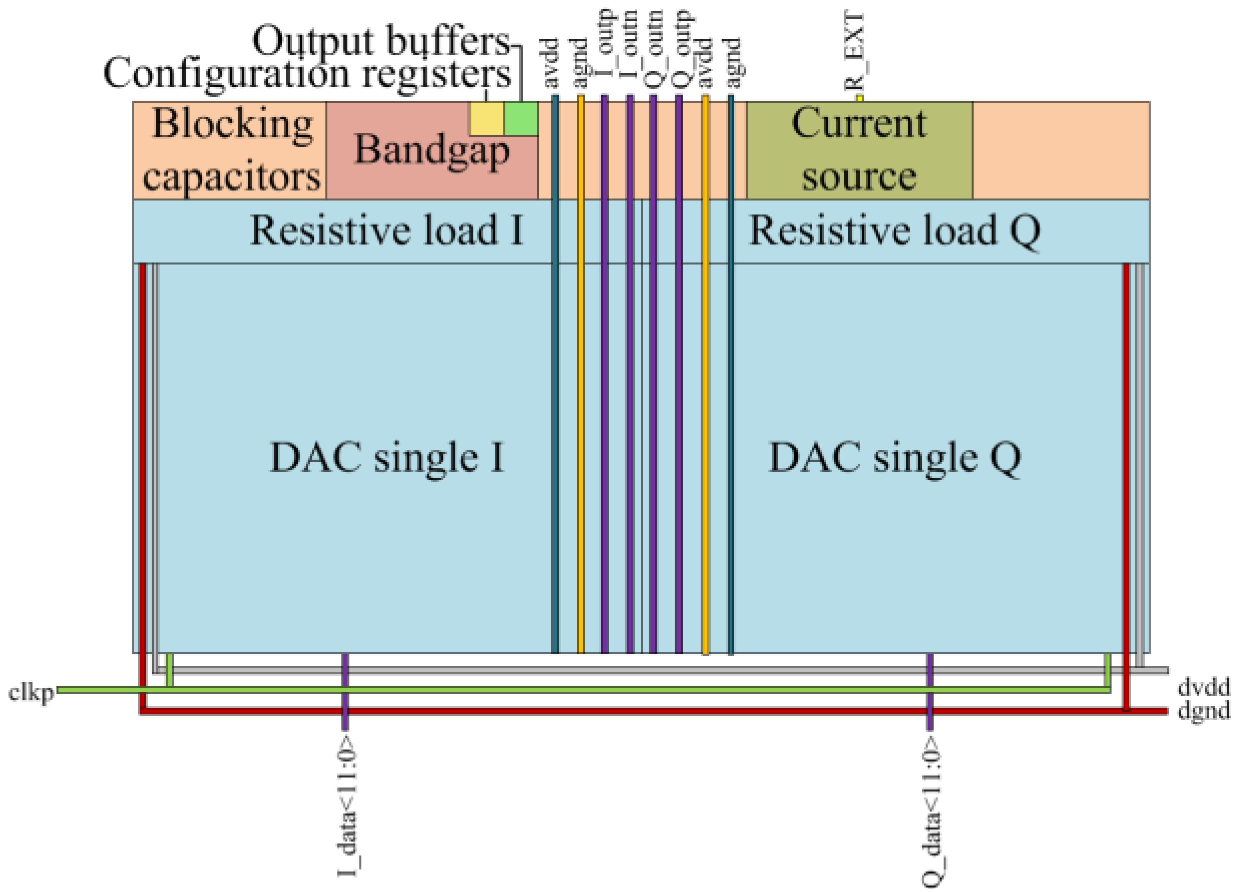

Figure 4: Layout floorplan with recommended routing

8 INTEGRATION GUIDELINES

8.1 PLACE AND ROUTE GUIDELINES

1) DAC should be placed on a top level chip corner section or close to one edge of the top level chip.
2) DAC analog outputs DAC_I_outp, DAC_I_outn, DAC_Q_outp, DAC_Q_outn should be connected to analog IO PADs or internal analog circuits (filter). IO PADs should not have an internal resistor to increase bandwidth.
3) DAC power supply and ground DAC_avdd, DAC_dvdd, DAC_agnd, DAC_dgnd should be connected to IO PADs.
4) Wiring of analog inputs should be symmetrical and as short as possible.
5) Noisy circuits should not place near DAC.
6) Minimum space 40 um between DAC and other circuits should be kept.
7) Minimum metal wiring width is 100 um for DAC_avdd, DAC_agnd. Multiple layers of metal can be used to reduce layout space.
8) Minimum metal wiring width is 10 um for DAC_dvdd, DAC_dgnd. Multiple layers of metal can be used to reduce layout space.
9) Allowable total resistance of DAC_avdd and DAC_agnd are 0.5 Ohm. Blocking capacitors should be added and placed as close as possible.
10) Allowable total resistance of DAC_dvdd and DAC_dgnd are 2 Ohm. Blocking capacitors should be added and placed as close as possible.

8.2 OPERATION GUIDELINES

1) Power supply decoupling should be done according the following figure. It is recommended the 100 nF capacitors to be placed as close as possible to the chip.

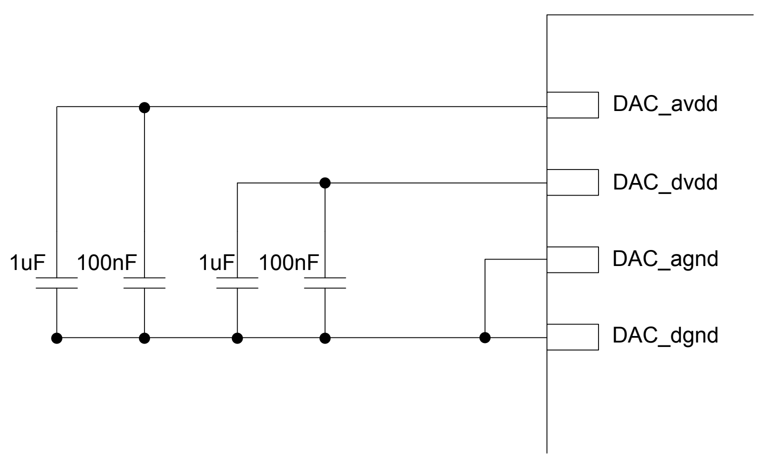

Figure 5: Power supply decoupling

9 OPERATION CHARACTERISTICS

9.1 TECHNICAL CHARACTERISTICS

Technology ____ TSMC CMOS 65 nm
Status ____ silicon proven
Area ____ 0.66 mm^2

9.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd_a}= 2.25÷2.75 V, V_{dd_d}= 1.08÷1.32 V and T_j= +27 °C, typical values are at V_{dd_a}= 2.5 V, V_{dd_d}= 1.2 V and T_j= 27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Operating temperature range	T_j	-	-40	27	+85	°C
Power supply requirements						
Analog supply voltage	V_{dd_a}	-	2.25	2.5	2.75	V
Digital supply voltage	V_{dd_d}	-	1.08	1.2	1.32	V
Analog current consumption in normal mode	I_{ACN}	$A_{IOUT\ p-p}$= 20.48 mA F_S= 140 MSPS	-	40.4	-	mA
Analog current consumption in pause mode	I_{ACP}	$A_{IOUT\ p-p}$= 20.48 mA F_S= 140 MSPS	-	40	-	mA
Digital current consumption in normal mode	I_{DCN}	$A_{IOUT\ p-p}$= 20.48 mA F_S= 140 MSPS	-	7.6*	-	mA
Digital current consumption in pause mode	I_{DCP}	F_S= 140 MSPS	-	60*	-	uA
Current consumption in standby mode	I_S	-	-	3*	-	uA
Total power consumption in normal mode	P_{CN}	$A_{IOUT\ p-p}$= 20.48 mA F_S= 140 MSPS $P_{ACN} + P_{DCN}$	-	110.2	-	mW
Total power consumption in pause mode	P_{CP}	$A_{IOUT\ p-p}$= 20.48 mA F_S= 140 MSPS $P_{ACP} + P_{DCP}$	-	100	-	mW
DC accuracy						
Resolution	N	-	-	12	-	bit
Differential nonlinearity	DNL	-	-	0.18*	-	LSB
Integral nonlinearity	INL	-	-	0.50*	-	LSB
Offset error	OE	-	-	0.1*	-	LSB
Gain error	GE	-	-	0.3*	-	LSB
Digital inputs						
Input logic coding			Offset binary			code
High level input voltage	V_{IH}	-	$0.7V_{dd\_d}$*	-	-	V
Low level input voltage	V_{IL}	-	-	-	$0.3V_{dd\_d}$*	V

Table “Electrical characteristics” (continue)

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Analog outputs						
Differential full-scale output current range	$A_{IOUT\ p\text{-}p}$	DAC_load_mode<1:0> = “0x”, DAC_CC<4:0>= “00000”	-	2.56*	-	mA
		DAC_load_mode<1:0> = “0x” DAC_CC<4:0>= “11111”	-	22.4*	-	mA
Differential full-scale output voltage range	$A_{VOUT\ p\text{-}p}$	DAC_load_mode<1:0> = “10” DAC_CC<4:0>= “00000”	-	0.256*	-	V
		DAC_load_mode<1:0> = “10” DAC_CC<4:0>= “11111”	-	2.240*	-	V
		DAC_load_mode<1:0> = “11” DAC_CC<4:0>= “00000”	-	0.128*	-	V
		DAC_load_mode<1:0> = “11” DAC_CC<4:0>= “11111”	-	1.120*	-	V
Output resistance	R_{OUT}	-	-	200*	-	kOhm
Output settling time	t_S	accuracy 0.1% code from 0 to FFF	-	1.2*	-	ns
Output rise time	t_R	from 10% to 90%	-	130*	-	ps
Output fall time	t_F	from 90% to 10%	-	110*	-	ps
Digital latency	L	-	-	1	-	clock cycles
Timing information						
Sampling rate	F_S	-	-	-	140	MSPS
Duty cycle	S	-	45	50	55	%
Dynamic characteristic at F_S= 50 MSPS and $A_{VOUT\ p\text{-}p}$= 1.28 V						
Noise spectral density	NSD	Fin= 5 MHz	143.4	143.9	144.6	dBm/Hz
		Fin= 10 MHz	140.5	142.5	144.0	dBm/Hz
		Fin= 20 MHz	138.1	140.0	143.5	dBm/Hz
Spurious-free dynamic range	SFDR	Fin= 5 MHz	64.4	68.1	72.9	dB
		Fin= 10 MHz	59.0	65.5	70.1	dB
		Fin= 20 MHz	53.0	61.1	64.7	dB
Dynamic characteristic at F_S= 100 MSPS and $A_{VOUT\ p\text{-}p}$= 1.28 V						
Noise spectral density	NSD	Fin= 5 MHz	144.0	144.7	145.2	dBm/Hz
		Fin= 10 MHz	143.7	144.5	145.0	dBm/Hz
		Fin= 20 MHz	142.7	144.2	145.0	dBm/Hz
		Fin= 30 MHz	142.9	144.0	144.5	dBm/Hz
Spurious-free dynamic range	SFDR	Fin= 5 MHz	64.8	69.5	73.8	dB
		Fin= 10 MHz	63.7	68.3	72.6	dB
		Fin= 20 MHz	62.3	64.4	65.4	dB
		Fin= 30 MHz	60.1	63.6	66.3	dB
Dynamic characteristic at F_S= 140 MSPS and $A_{VOUT\ p\text{-}p}$= 1.28 V						
Noise spectral density	NSD	Fin= 5 MHz	144.3	144.6	145.0	dBm/Hz
		Fin= 10 MHz	143.8	144.3	145.2	dBm/Hz
		Fin= 20 MHz	143.6	144.4	145.3	dBm/Hz
		Fin= 30 MHz	142.7	143.9	144.8	dBm/Hz
		Fin= 40 MHz	140.8	142.9	143.8	dBm/Hz
Spurious-free dynamic range	SFDR	Fin= 5 MHz	65.0	70.8	73.9	dB
		Fin= 10 MHz	63.3	69.2	74.0	dB
		Fin= 20 MHz	60.5	62.7	65.5	dB
		Fin= 30 MHz	60.1	61.6	63.2	dB
		Fin= 40 MHz	58.5	64.5	66.0	dB

*-according to modeling

10 TYPICAL CHARACTERISTICS

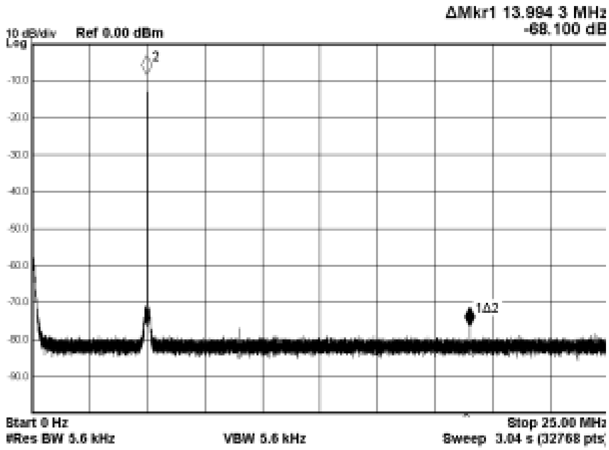

Figure 6: Spectrum with F_S= 50 MSPS, Fin= 5 MHz and $A_{VOUT\ p\text{-}p}$= 1.28 V

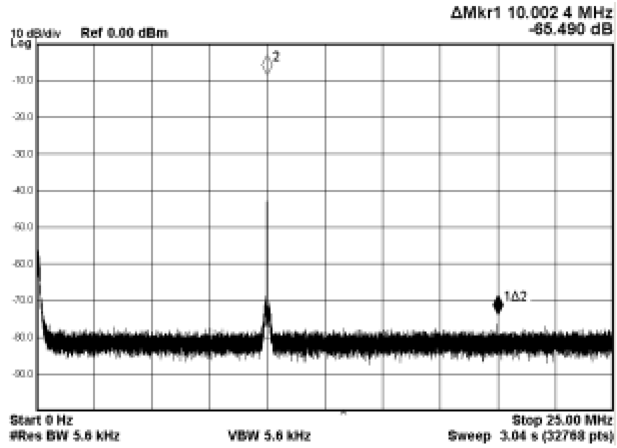

Figure 7: Spectrum with F_S= 50 MSPS, Fin= 10 MHz and $A_{VOUT\ p\text{-}p}$= 1.28 V

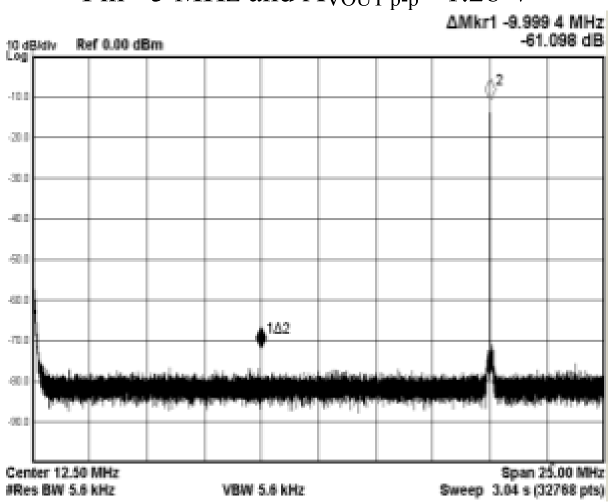

Figure 8: Spectrum with F_S= 50 MSPS, Fin= 20 MHz and $A_{VOUT\ p\text{-}p}$= 1.28 V

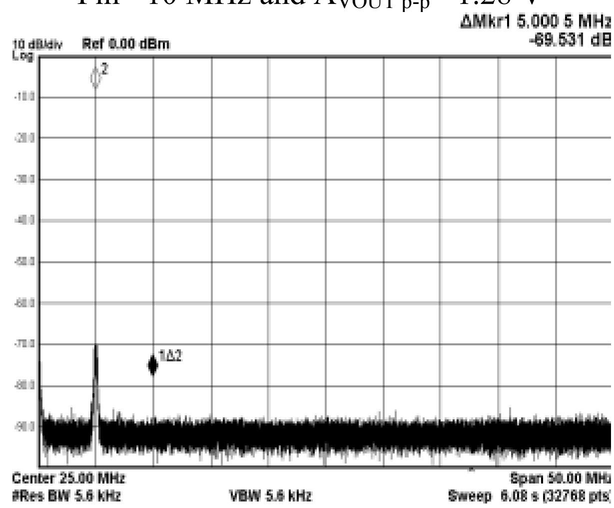

Figure 9: Spectrum with F_S= 100 MSPS, Fin= 5 MHz and $A_{VOUT\ p\text{-}p}$= 1.28 V

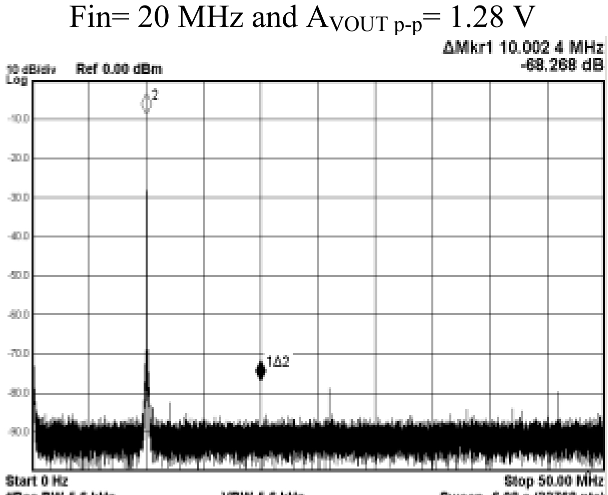

Figure 10: Spectrum with F_S= 100 MSPS, Fin= 10 MHz and $A_{VOUT\ p\text{-}p}$= 1.28 V

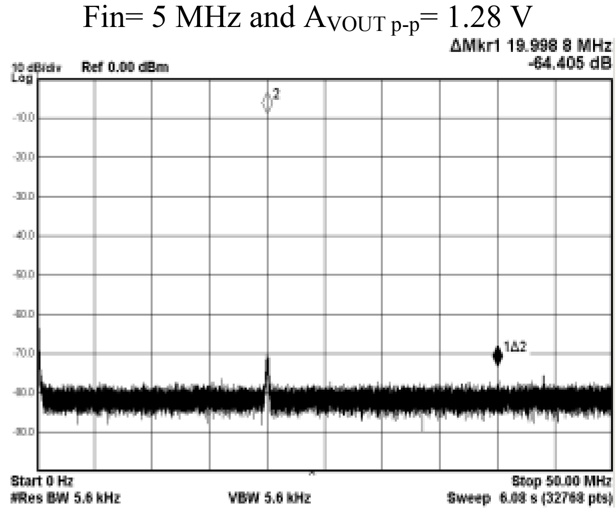

Figure 11: Spectrum with F_S= 100 MSPS, Fin= 20 MHz and $A_{VOUT\ p\text{-}p}$= 1.28 V

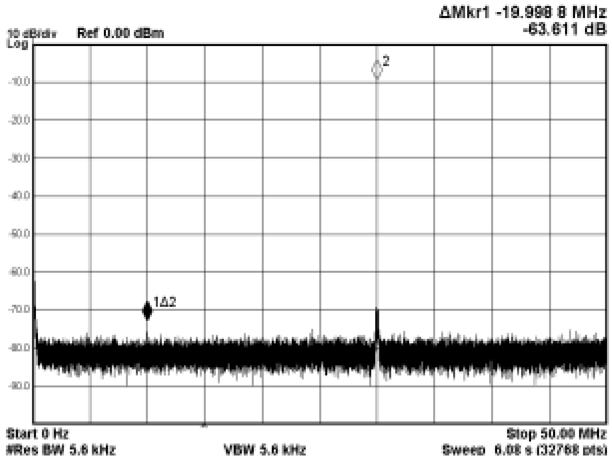

Figure 12: Spectrum with F_S= 100 MSPS, Fin= 30 MHz and $A_{VOUT\ p\text{-}p}$= 1.28 V

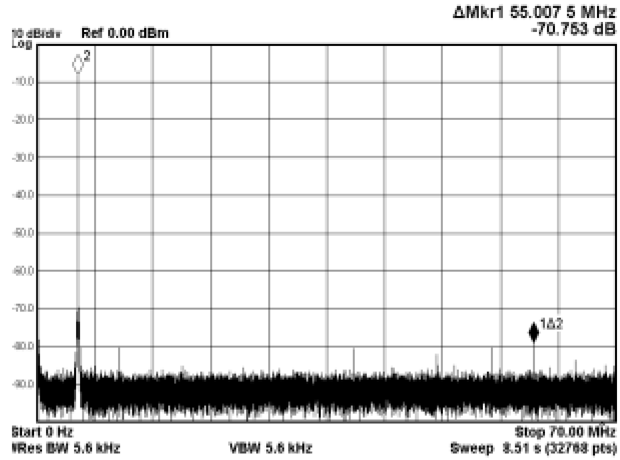

Figure 13: Spectrum with F_S= 140 MSPS, Fin= 5 MHz and $A_{VOUT\ p\text{-}p}$= 1.28 V

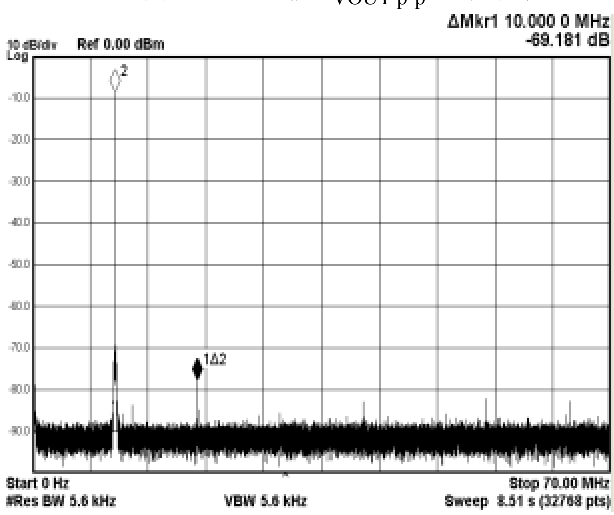

Figure 14: Spectrum with F_S= 140 MSPS, Fin= 10 MHz and $A_{VOUT\ p\text{-}p}$= 1.28 V

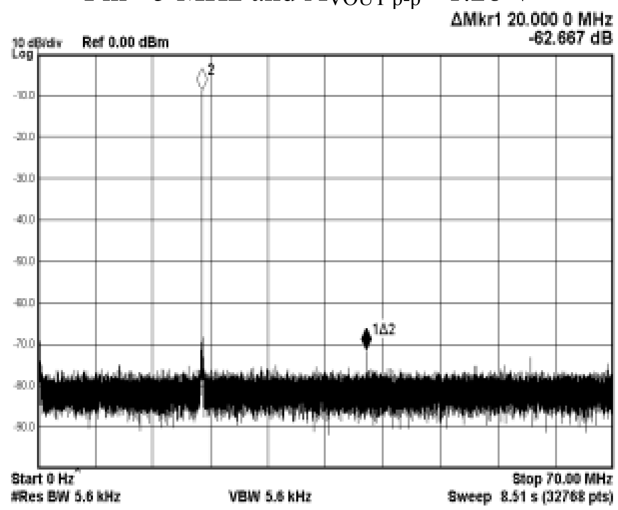

Figure 15: Spectrum with F_S= 140 MSPS, Fin= 20 MHz and $A_{VOUT\ p\text{-}p}$= 1.28 V

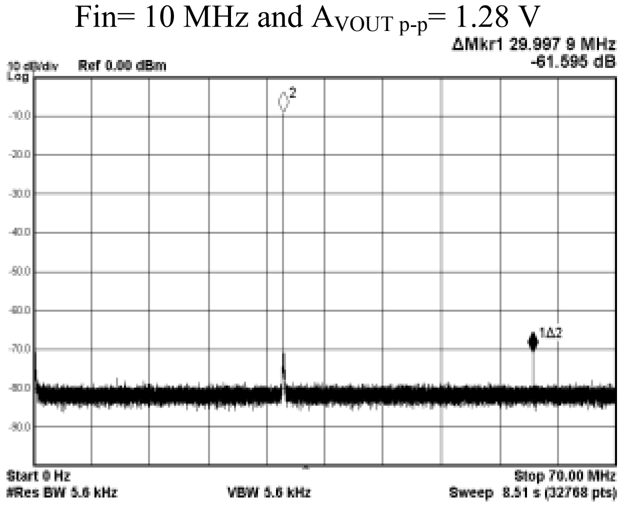

Figure 16: Spectrum with F_S= 140 MSPS, Fin= 30 MHz and $A_{VOUT\ p\text{-}p}$= 1.28 V

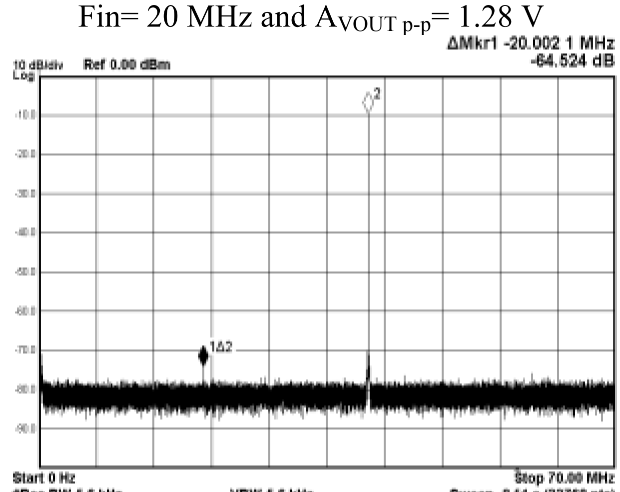

Figure 17: Spectrum with F_S= 140 MSPS, Fin= 40 MHz and $A_{VOUT\ p\text{-}p}$= 1.28 V

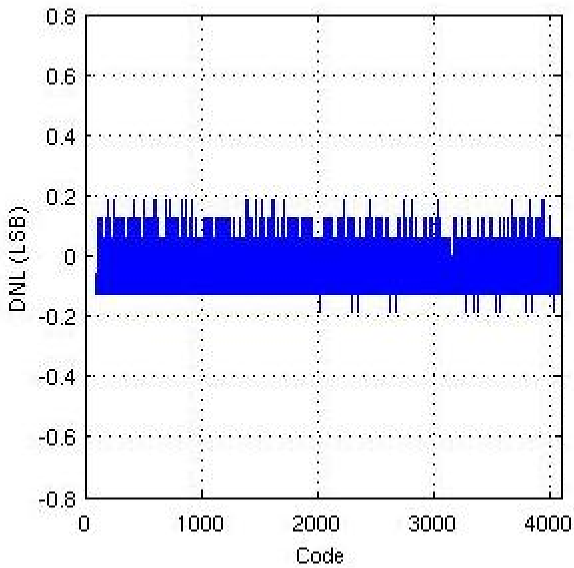

Figure 18: Differential nonlinearity

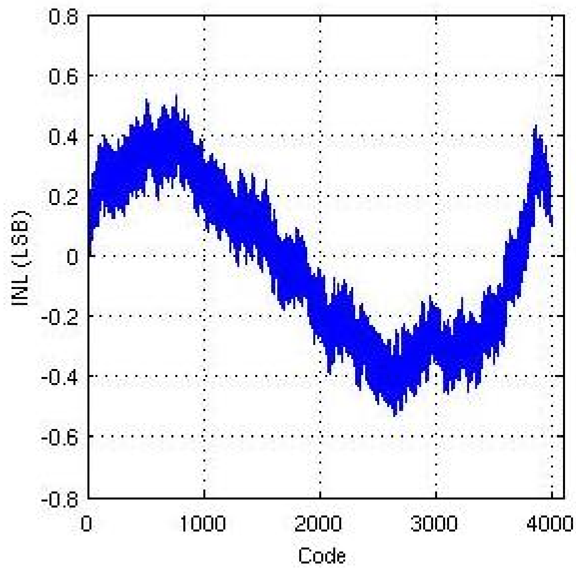

Figure 19: Integral nonlinearity

11 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation