10-bit CS HS DAC

SPECIFICATION

1. FEATURES

- TSMC CMOS 90 nm
- Resolution 10-bit
- Sampling rate 100 MSPS
- External reference voltage
- 1.5 to 18.5 mA differential current output
- Power dissipation: 3.1 mW…35.5 mW (depending on level of output current)
- High spurious free dynamic range performance up to 25 MHz output
- Reset mode
- Standby current - 10 uA
- Small area - 0.0984 mm^2
- Portable to other technologies (upon request)

2. APPLICATION

- Wireless infrastructures
- Broadband communications
- Picocell, femtocell base stations
- Medical instrumentation
- Ultrasound transducer excitation
- Signals and arbitrary waveform generators

3. OVERVIEW

The 10-bit dual high-speed 100 MHz DAC is based on current steering architecture, which provides high-speed conversion rate and good dynamic performance. DAC consists of four principal blocks: adjustable bias, control logic, current source array and current output switches. Device has a feature of adjusting output current, output cascade transistors bias voltage (see figure 2), and entering sleep mode, turning device off. DAC requires 1V digital supply, 1.8V digital and analog supply, and digital and analog ground to work properly.

The DAC provides differential current outputs to support single ended or differential configurations. The output currents can be used to drive directly two external resistive loads to obtain two complementary single-ended output voltages, or can be used to drive an external transformer (or amplifier) to obtain a single-ended output voltage. The DAC uses a segmented thermometer decoded current steering architecture, with 8 thermometer and 2 binary bits to achieve simultaneously high update rate and good dynamic characteristics. External voltage reference is used to set the full-scale current of the DAC and operating points of subcircuits.

The block is designed on TSMC CMOS 90 nm technology.

4. STRUCTURE

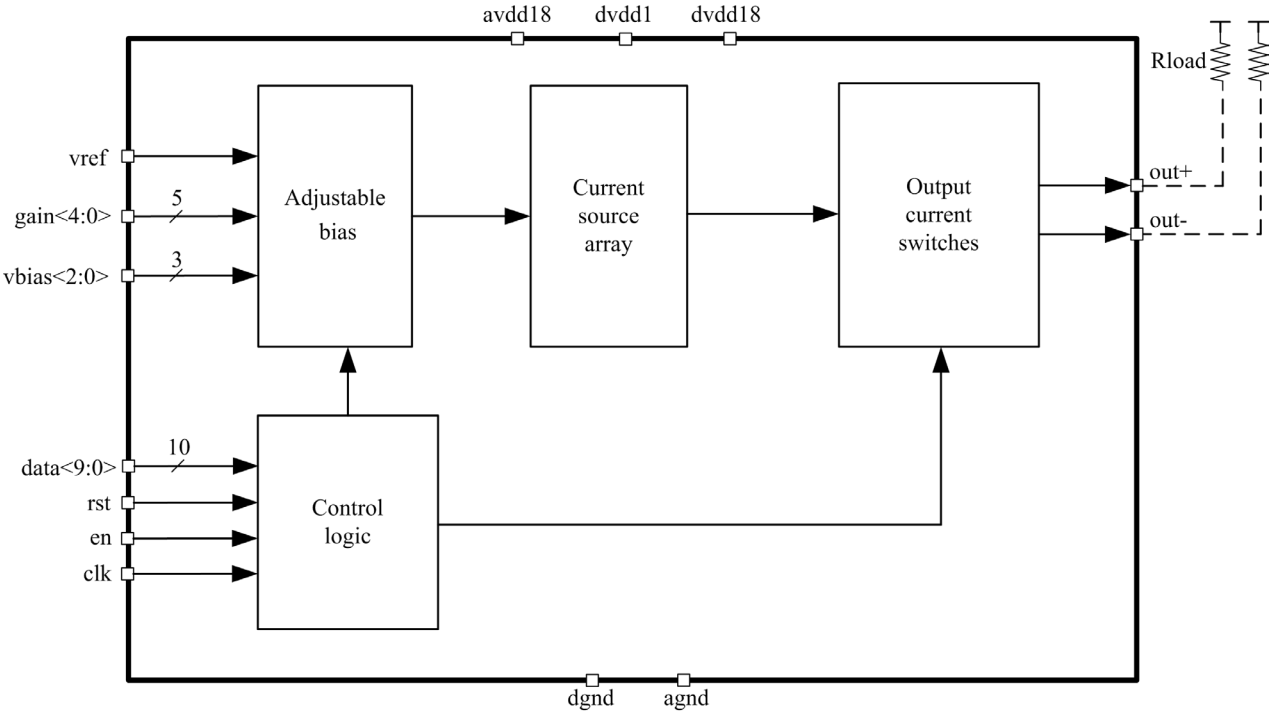

Figure 1: 10-bit CS HS DAC block diagram

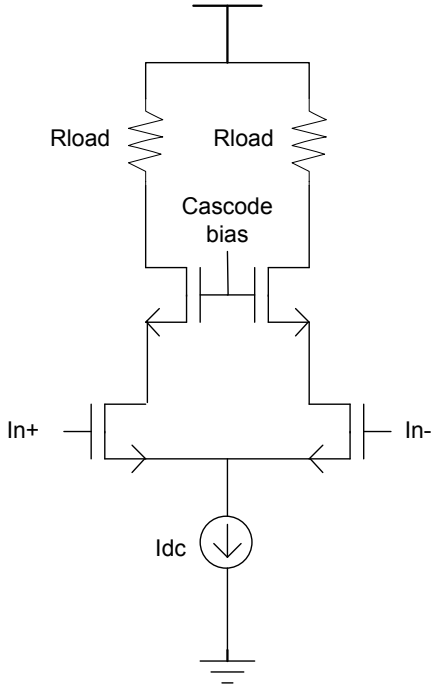

Figure 2: Current cell simplified view

5. PIN DESCRIPTION

Name	Direction	Description
vref	I	Reference voltage input
clk	I	Clock input (1 V)
en	I	Enable input (1 V)
rst	I	Reset enable input (data inputs are set to middle scale value; 1 V)
out-	O	Negative current output
out+	O	Positive current output
data<9:0>	I	Input data line (1 V)
gain<4:0>	I	DAC output current adjustment: “00000” 1.1 mA ….. ~ step 0.54 mA “11111” 18.5 mA
vbias<2:0>	I	Cascode transistors bias input (sets the bias at cascode’s gates; 1 V)
avdd18	I/O	Analog block supply voltage (1.8 V)
dvdd18	I/O	Digital blocks supply voltage (1.8 V)
dvdd1	I/O	Digital blocks supply voltage (1 V)
dgnd	I/O	Analog blocks ground
agnd	I/O	Digital blocks ground

6. LAYOUT DESCRIPTION

CS HS DAC layout dimensions are given in the next tables:
1. Bias + control logic
2. Current source array + current output switches

Table 1: Bias + control logic dimensions

Dimension	Value	Unit
Height	112	um
Width	75	um

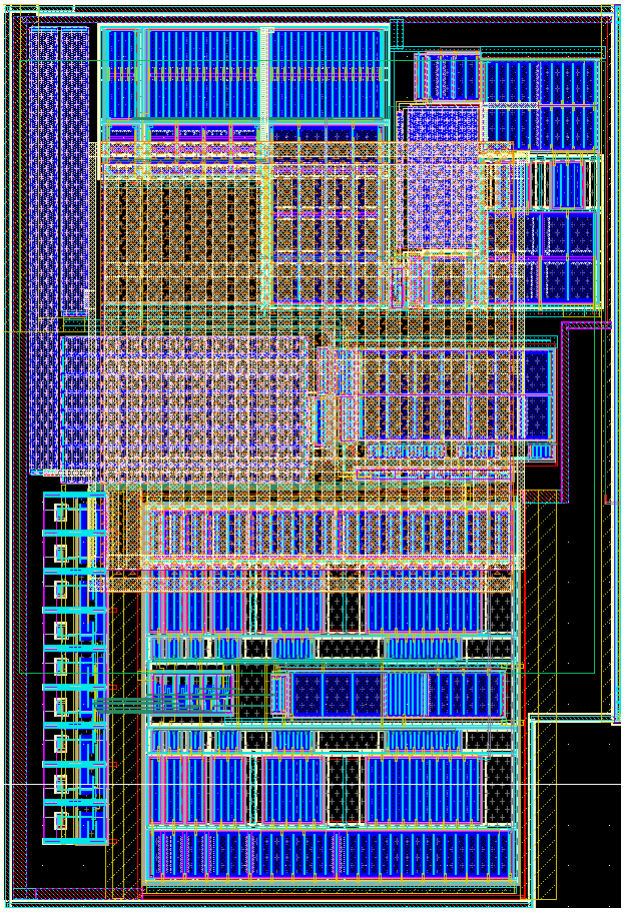

Figure 3: Adjustable bias and control logic layout

Table 2: DAC core array dimensions

Dimension	Value	Unit
Height	180	um
Width	500	um

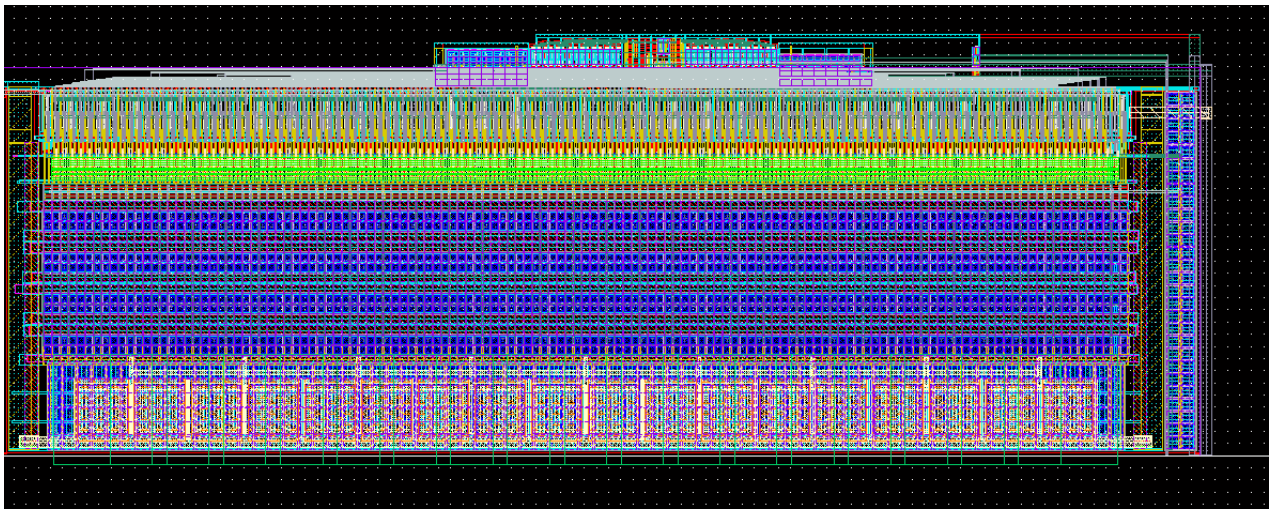

Figure 4: Current source array + current output switches dimensions

7. OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC CMOS 90nm
Status _____ silicon proven
Area _____ 0.0984 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd18} = 1.7 ÷ 1.9 V, V_{dd}=0.9 ÷ 1.1 V and T_j = -40 ÷ +125 °C. Typical values are at V_{dd18} = 1.8 V, V_{dd} = 1 V, T_j = +27 °C, Rload = 25 Ohm, Fclk = 50 MHz and registers values gain<4:0> = "11111", vbias<2:0> = "110" unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Analog and digital supply voltage	V_{dd18}	-	1.7	1.8	1.9	V
Analog and digital supply voltage	V_{dd}	-	0.9	1	1.1	V
Operating temperature range	T_j	-	-40	27	+125	°C
Resolution	N	-	-	10	-	bit
Spurious-free dynamic range	SFDR	Measured in Nyquist band Fin<=25 MHz	60	60	66	dB
Sampling rate	F_s	-	1	-	100	MSPS
DNL	DNL	-	-	±1	-	LSB
INL	INL	-	-	±1	-	LSB
Output current	I_{out}	gain<4:0> = "00000"	-	1.50	-	mA
		gain<4:0> = "10000"	-	9.74	-	
		gain<4:0> = "11111"	-	18.50	-	
Reference voltage	V_{ref}	-	-	1.2	-	V
Output compliance range	$V_{out\ compl}$	-	1	-	2	V
Clock duty cycle	CDC	-	45	50	55	%
Startup time	T_{start}	From En = "0" to En = "1", Bias+DAC core	-	3	-	us
Setup time	T_{st}	-	-	0.5	-	ns
Hold time	T_h	-	-	0.5	-	ns
Power consumption	P_{diss}	gain<4:0> = "00000"	-	3.1	-	mW
		gain<4:0> = "10000"	-	16.9	-	
		gain<4:0> = "11111"	-	35.5	-	

Table “Electrical characteristics” (continue)

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
DAC core power consumption	Pdaccore	gain<4:0> = “00000”	-	2.7	-	mW
		gain<4:0> = “10000”	-	15.6	-	
		gain<4:0> = “11111”	-	33.3	-	
Bias power consumption	Ppwbias	gain<4:0> = “00000”	-	0.4	-	mW
		gain<4:0> = “10000”	-	1.4	-	
		gain<4:0> = “11111”	-	2.16	-	
Standby current	I_{sb}	-	-	10	-	uA
Input high-logic level	V_{IH}	-	$0.7V_{dd}$	-	-	V
Input low-logic level	V_{IL}	-	-	-	$0.3V_{dd}$	V

In this mode, an external reference resistor must be used to define the internal reference current as represented in figure below. The internal reference current IREF is defined as:

- to program output current you need to adjust registers gain<4:0>. The output current is defined as the sum of binary weighted values;
- maximum output current is set by entering all ones to gain register (gain<4:0> = “11111”) and equals approximately 18.5 mA;
- minimum current is by entering all zeros to gain register (gain<4:0> = “00000”) and equals approximately 1.1 mA. It is default current.

Current can be gradually adjusted by increasing gain code. LSB step value is approximately equal 0.54 mA.

8. DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

1. From version 1.0:
   - Section 1 updated (refer to page 1)
   - Subsection 7.1 updated (refer to page 5)
2. From version 1.1:
   - Section 1 updated (refer to page 1)
   - Subsection 7.1 updated (refer to page 6)