12-bit 1-channel 1 MSPS R/2R DAC

SPECIFICATION

1. FEATURES

- TSMC CMOS 90 nm
- Resolution 12-bit
- 1 channel
- Different power supplies for digital (1.0 V) and analog (1.8 V) parts
- Sampling rate up to 1 MSPS
- Standby mode (current consumption 180 nA)
- Resistive load from 5 kOhm
- Power dissipation 1.53 mW
- Differential nonlinearity 0.74 LSB
- Integrated nonlinearity 1.20 LSB
- Time setup 278 ns
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2. APPLICATION

- Industrial process control
- Automated test equipment
- Digital calibration
- Data acquisition system
- Motion control system

3. OVERVIEW

12-bit 1MSPS R/2R DAC contains four main blocks: reference voltage source, bias voltage source, DAC core and control digital module. DAC core consist of the R/2R matrix and output operational class AB amplifier. Digital control register adj<15:4> sets optimal mode. It corrects output buffers current, common mode and output signal swing. DAC requires 1.62 ÷ 1.98 V (port V_{dd18}) analog supply voltage and 0.9 ÷ 1.1 V (port V_{dd}) digital supply voltage.
The block is designed on TSMC CMOS 90 nm technology.

4. STRUCTURE

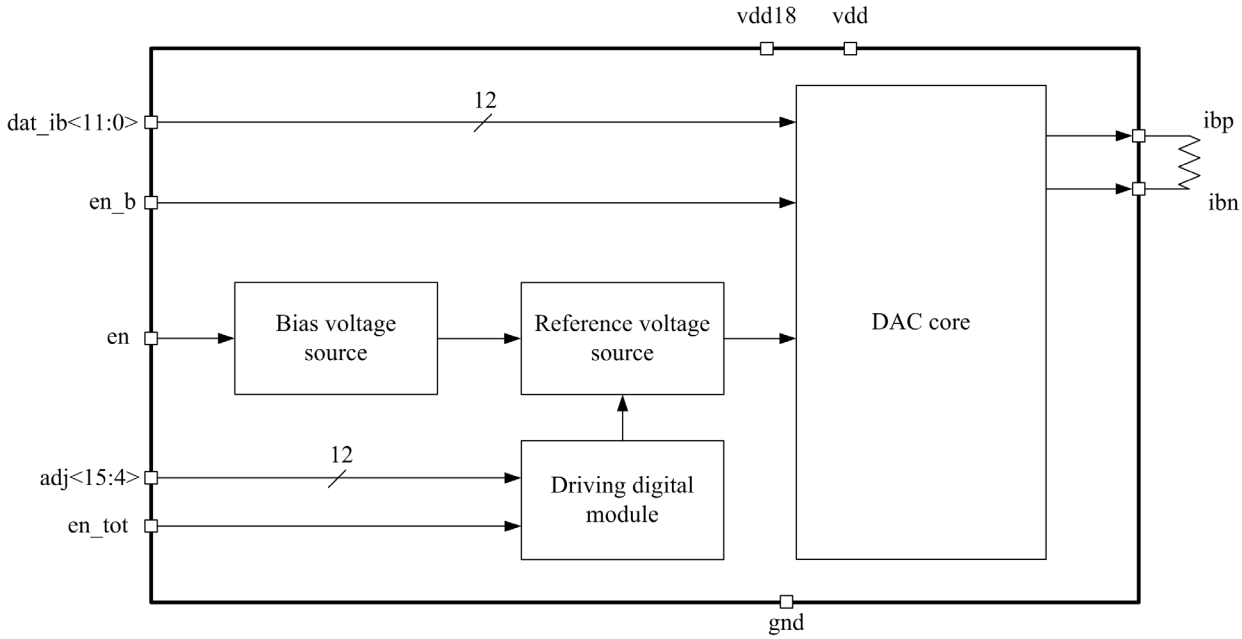

Figure 1: 12-bit R/2R 1MSPS R2/R DAC structure

5. PIN DESCRIPTION

Name	Direction	Description
en_tot	I	Global enable
en_b	I	Enable conversion
en	I	Enable reference voltage source
ibp	O	Differential output
ibn		
dat_ib<11:0>	I	Input data
adj<15:4>	I	Digital adjusting DAC register
vdd18	I/O	Analog blocks supply voltage 1.8 V
vdd	I/O	Digital blocks supply voltage 1 V
gnd	I/O	Ground

Table 1: DAC adjusting register description

Bit range adj<15:4> register	Function
adj<15:12>	Adjustment common mode of input signal
adj<11:8>	Adjustment amplitude of output signal
adj<7:4>	Adjustment bias current of output buffer

6. LAYOUT DESCRIPTION

12-bit 1MSPS R2/R DAC layout dimensions are given in table 2.

Table 2: Block dimensions

Dimension	Value	Unit
Height	425	um
Width	580	um

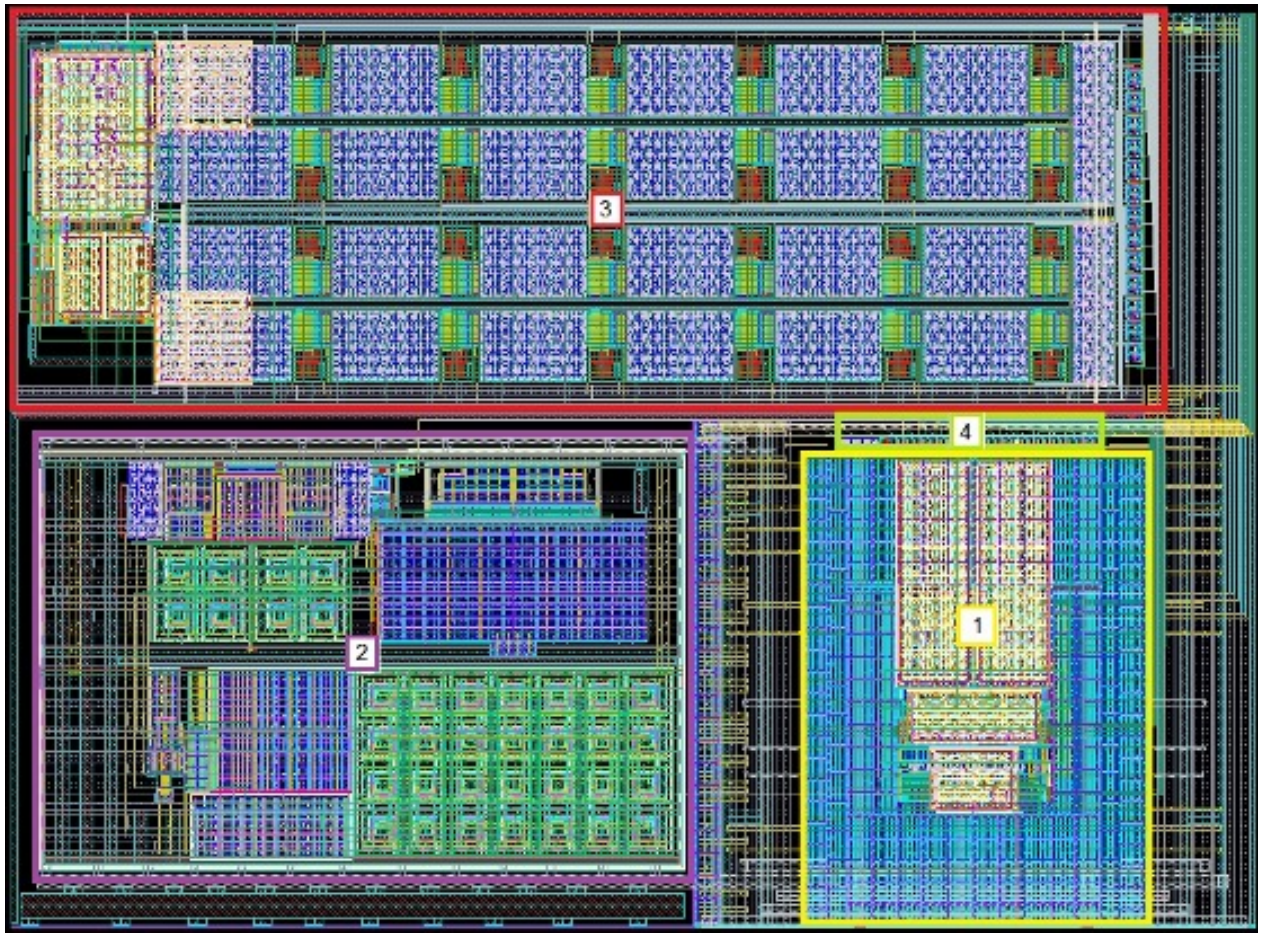

Figure 2: 12-bit 1MSPS R/2R DAC layout view

1. Bias voltage source
2. Reference voltage source
3. DAC core
4. Digital control module

7. OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 90nm
Status silicon proven
Area 0.246 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd18} = 1.62÷1.98 V, V_{dd} = 0.9÷1.1 V and T_j = -60÷ +125 °C, typical values are at V_{dd18} = 1.8 V, V_{dd} = 1 V and T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Analog blocks supply voltage	V_{dd18}	-	1.62	1.8	1.98	V
Digital blocks supply voltage	V_{dd}	-	0.9	1.0	1.1	V
Operating temperature range	T_j	-	-60	27	+125	°C
Resolution	N	-	-	12	-	bit
Resistive load	R_{load}	-	5	-	-	kOhm
Sampling rate	F_s	-	-	1	-	MSPS
Standby current	I_{st}	-	-	180	-	nA
Current consumption	I_{cn}	-	0.47	0.88	1.95	mA
Power consumption	P_{cn}	-	0.76	1.53	3.86	mW
Differential output voltage range	V_{dref}	-	1	1	2	V
Common mode of output signal	V_{cmout}	-	0.68	1	1.3	V
Maximum differential nonlinearity	DNL	F_s = 1 MSPS: adjust registers value : adj<15:4> = “100000000100”	0.52	0.74	0.93	LSB
Maximal integrated nonlinearity	INL		0.93	1.20	1.48	LSB
Offset error	OE		-8	0.88	8	LSB
Gain error	GE		-0.89	-0.17	0.89	LSB
Time setup	t_{set}		276	278	279	ns
Input high-logic level	V_{IH}	-	0.7	-	-	V
Input low-logic level	V_{IL}		-	-	0.3	V

8. TYPICAL CHARACTERISTICS

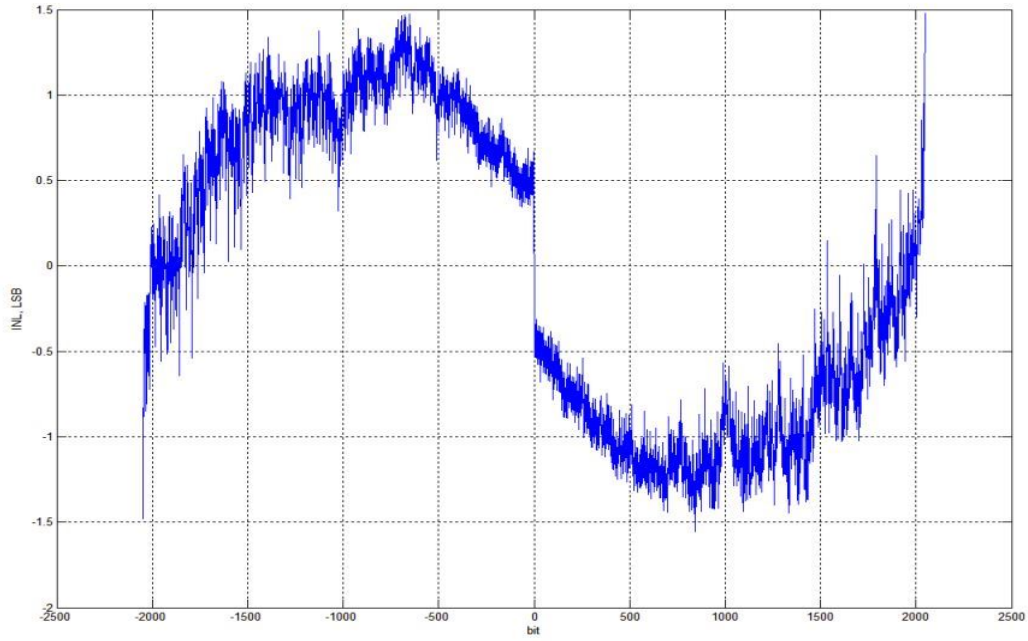

Figure 3: Integral nonlinearity, R_{load} = 5 kOhm

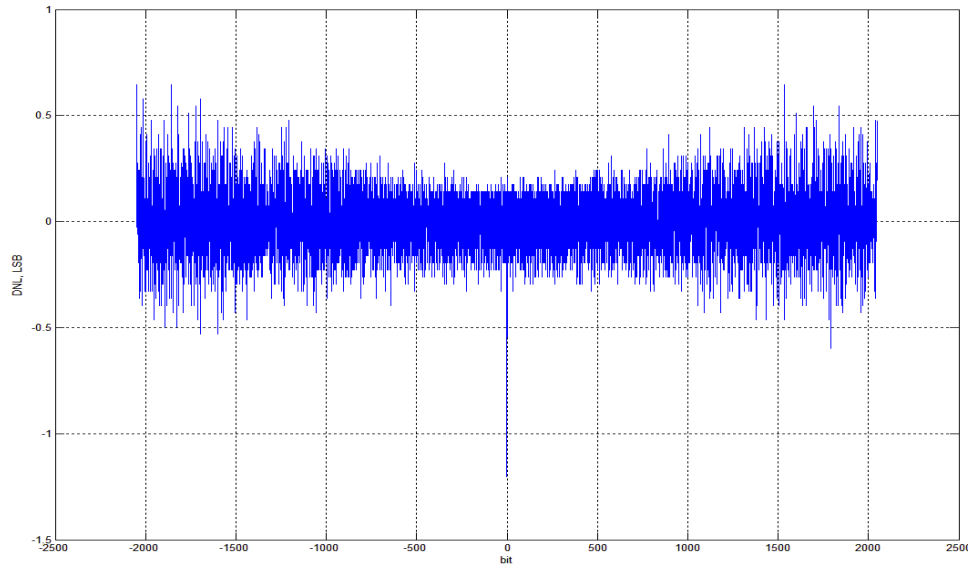

Figure 4: Differential nonlinearity, R_{load} = 5 kOhm

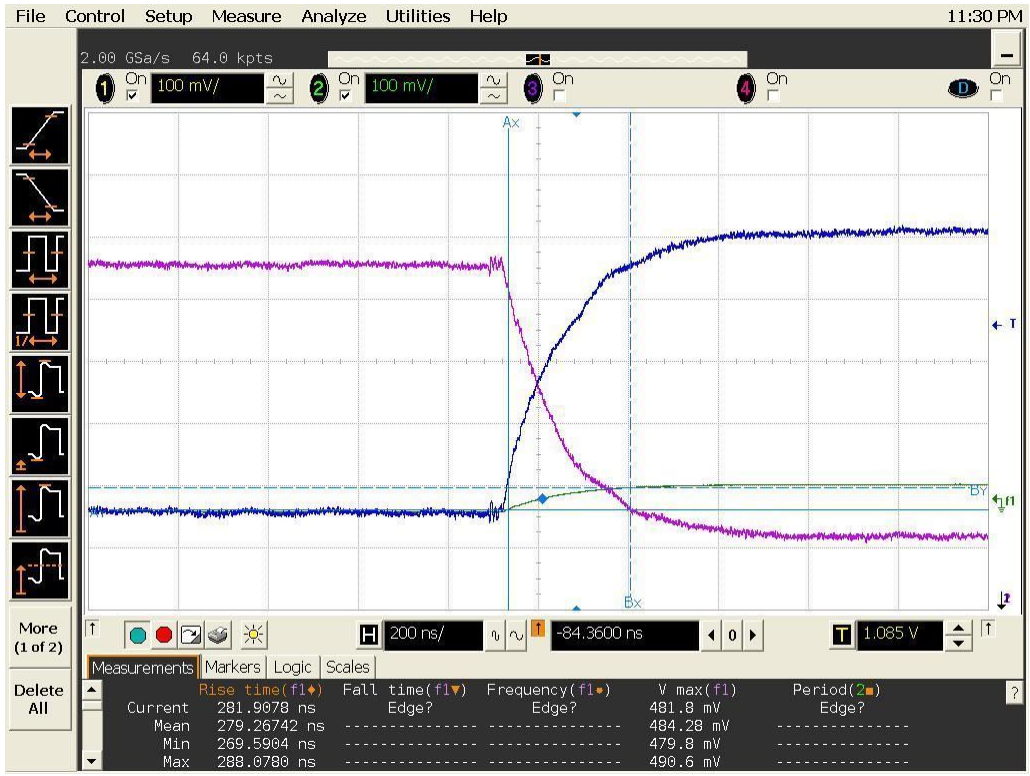

Figure 5: Settling time measurement

9. DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation