12-bit 16-channel R/2R DAC

SPECIFICATION

1 FEATURES

- Technology TSMC 90 nm MS CMOS
- R/2R architecture
- Resolution 12-bit
- 1 MHz sampling rate
- Different power supplies for digital (1.0 V) and analog (1.8 V) parts
- Standby mode (current consumption <650nA)
- 11.9 mW power dissipation
- 0.74 LSB maximum differential nonlinearity
- 1.20 LSB maximal integrated nonlinearity
- 278 ns time setup
- Small area
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Industrial process control
- Automated test equipment
- Digital calibration
- Data acquisition systems
- Motion control systems

3 OVERVIEW

The 16-channels 12-bit R/2R DAC contains a three principal blocks: adjustable bias, DAC core and logic block. DAC core consist of 16 identical R/2R DAC, each of which include differential R/2R ladder and output operational amplifier AB class. There is a possibility to turn off each output channels and whole scheme Digital control register adj<15:4> sets optimal mode by reducing current consumption. It corrects output buffers current, common mode and swing output signal. DAC requires 1.62 ÷ 1.98 V (port V_{dd18}) analog supply and 0.9 ÷ 1.1 B (port V_{dd}) digital supply.

4 STRUCTURE

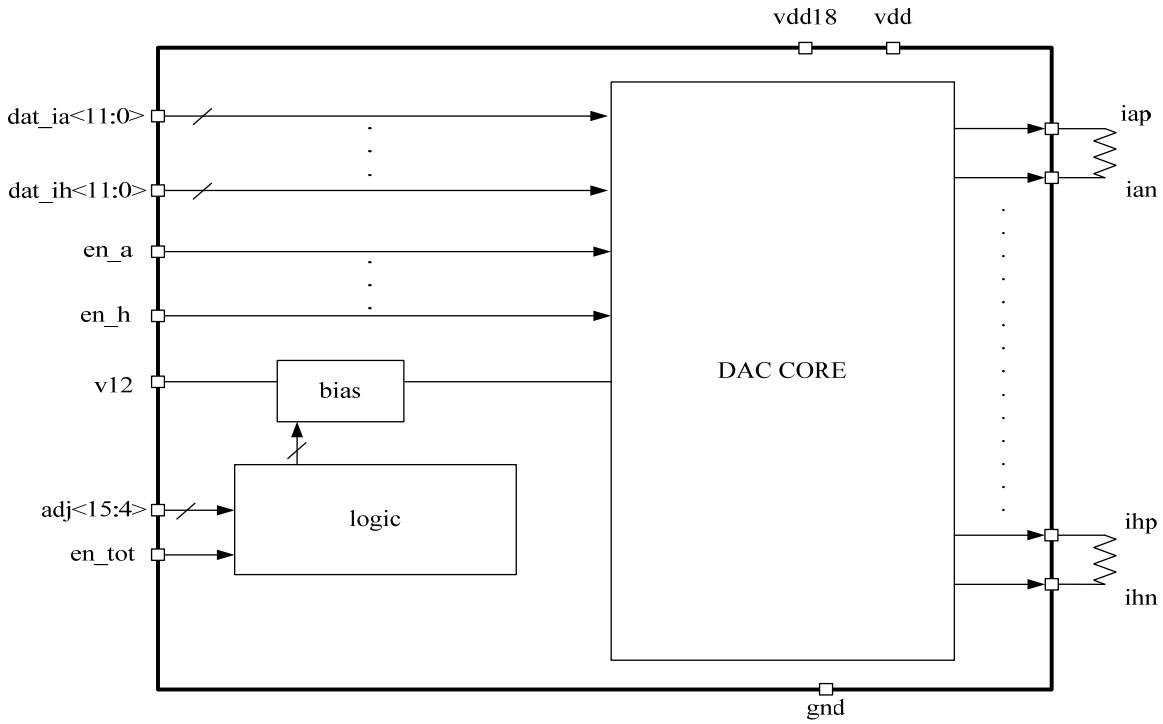

Figure 1: 12-bit R/2R DAC structure.

5 PIN DESCRIPTION

Name	Direction	Description
dat_ia<11:0>	I	Input data line channel ia
dat_qa<11:0>	I	Input data line channel qa
dat_ib<11:0>	I	Input data line channel ib
dat_qb<11:0>	I	Input data line channel qb
dat_ic<11:0>	I	Input data line channel ic
dat_qc<11:0>	I	Input data line channel qc
dat_id<11:0>	I	Input data line channel id
dat_qd<11:0>	I	Input data line channel qd
dat_ie<11:0>	I	Input data line channel ie
dat_qe<11:0>	I	Input data line channel qe
dat_if<11:0>	I	Input data line channel if
dat_qf<11:0>	I	Input data line channel qf
dat_ig<11:0>	I	Input data line channel ig
dat_qg<11:0>	I	Input data line channel qg
dat_ih<11:0>	I	Input data line channel ih
dat_qh<11:0>	I	Input data line channel qh
en_tot	I	Enable total
V12	I	1.2V Voltage reference
adj<15:4>	I	Digital adjusting DAC register
en_a	I	Enable channels ia and qa
en_b	I	Enable channel ib and qb
en_c	I	Enable channel ic and qc
en_d	I	Enable channel id and qd
en_e	I	Enable channel ie and qe
en_f	I	Enable channel if and qf
en_g	I	Enable channel ig and qg
en_h	I	Enable channel ih and qh
iap ian	O	Differential output channel ia
qap qan	O	Differential output channel qa
ibp ibn	O	Differential output channel ib
qbp qbn	O	Differential output channel qb
icp icn	O	Differential output channel ic
qcp qcn	O	Differential output channel qc
idp idn qdp qdn	O	Differential output channel id

Table 5.1 (continue).

Name	Direction	Description
iep ien	O	Differential output channel ie
qep qen	O	Differential output channel qe
ifp ifn	O	Differential output channel if
qfp qfn	O	Differential output channel qf
igp ign	O	Differential output channel ig
qgp qgn	O	Differential output channel qg
ihp ihn	O	Differential output channel ih
qhp qhn	O	Differential output channel qh
vdd18	I/O	Analog blocks supply voltage (1.8 V)
vdd	I/O	Digital blocks supply voltage (1 V)
gnd	I/O	Ground

Table 1: Description of DAC Adjusting Register signals.

Bit range of register ADJ<15:4>	Function
ADJ<15:12>	Adjusting common mode of input signal
ADJ<11:8>	Adjusting amplitude of output signal
ADJ<7:4>	Adjusting bias current of output buffer

6 LAYOUT DECRIPTION

Digital-to-analog converter layout dimensions are given in the table 2.

Table 2: Block dimensions.

Dimension	Value	Unit
Height	738	µm
Width	2386	µm

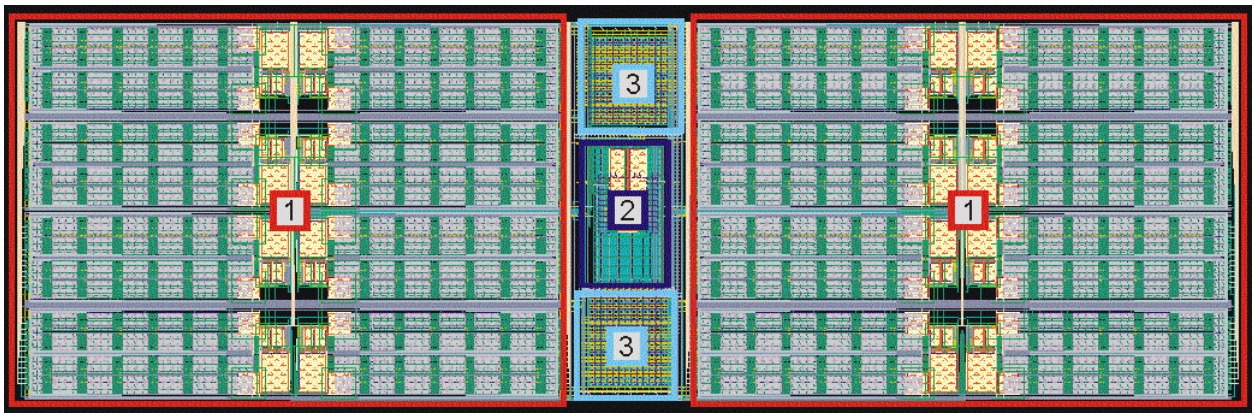

Figure 2: 12-bit R/2R DAC layout.

1. Adjustable bias
2. DAC core
3. Filtering capacitors

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC 90nm CMOS
Status _____ pre-silicon verification
Area _____ 1.76 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd18} = 1.62 ÷ 1.98 V, V_{dd} = 0.9 ÷ 1.1 V and T = -60 ÷ 125°C, typical values are at V_{dd18} = 1.8V, V_{dd} = 1V, T = 27°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Operating temperature range	T	-	-60	27	+125	°C
Analog blocks supply voltage	V_{dd18}	-	1.62	1.8	1.98	V
Digital blocks supply voltage	V_{dd}	-	0.9	1.0	1.1	V
Reference voltage	V_{ref}	-	1.08	1.2	1.32	V
Resolution	N	-	-	12	-	bit
Clock rate	F_{clk}	-	-	1	-	MSPS
Stand-by current	I_{st}	-	-	650	-	nA
Power consumption	P_{cn}	-	4.34	11.9	43.04	mW
Current consumption	I_{cn}	-	2.68	6.6	21.74	mA
Differential output voltage range	V_{dref}	-	1.04	1.04	2.0	mV
Common mode of output signal	V_{cmout}	-	0.68	1.0	1.3	mV
Maximum differential nonlinearity	DNL	F_{clk}=1 MHz, adjust registers value adj<15:4>=100000000100	0.52	0.74	0.93	LSB
Maximal integrated nonlinearity	INL		0.93	1.20	1.48	LSB
Offset error	OE		-8.0	0.88	8.0	LSB
Gain error	GE		-0.89	-0.17	0.89	LSB
Time setup	t_{set}		276	278	279	ns
High Level Input Voltage	V_{IH}	For digital inputs	0.7	-	-	V
Low Level Input Voltage	V_{IL}		-	-	0.3	V

8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation