10-bit DAC

SPECIFICATION

1. FEATURES

- SMIC EEPROM CMOS 0.18 um
- Resolution 10-bit
- 100 MHz update rate
- High spurious free dynamic range performance up to 25 MHz output
- Adjustable output current (from 1.3 mA to 21 mA)
- Standby mode (current consumption less than 200 nA)
- Portable to other technologies (upon request)

2. APPLICATION

- Wireless infrastructures
- Picocell, femtocell base stations
- Medical instrumentation
- Ultrasound transducer excitation
- Signals generators, arbitrary waveform generators

3. OVERVIEW

The 10-bit dual high-speed DAC is based on current steering architecture, which provides high-speed conversion rate and good dynamic performance. DAC consists of three principal blocks: adjustable reference voltage and current generator, decoding logic, current source and output switches array. Device has a feature of adjusting output current and entering sleep mode, turning the device off. DAC requires 1.8 V analog and digital supply, and digital and analog ground to work properly. Pins dac<2:0> adjust DAC output current.
The block is designed on SMIC EEPROM CMOS 0.18 um technology.

4. STRUCTURE

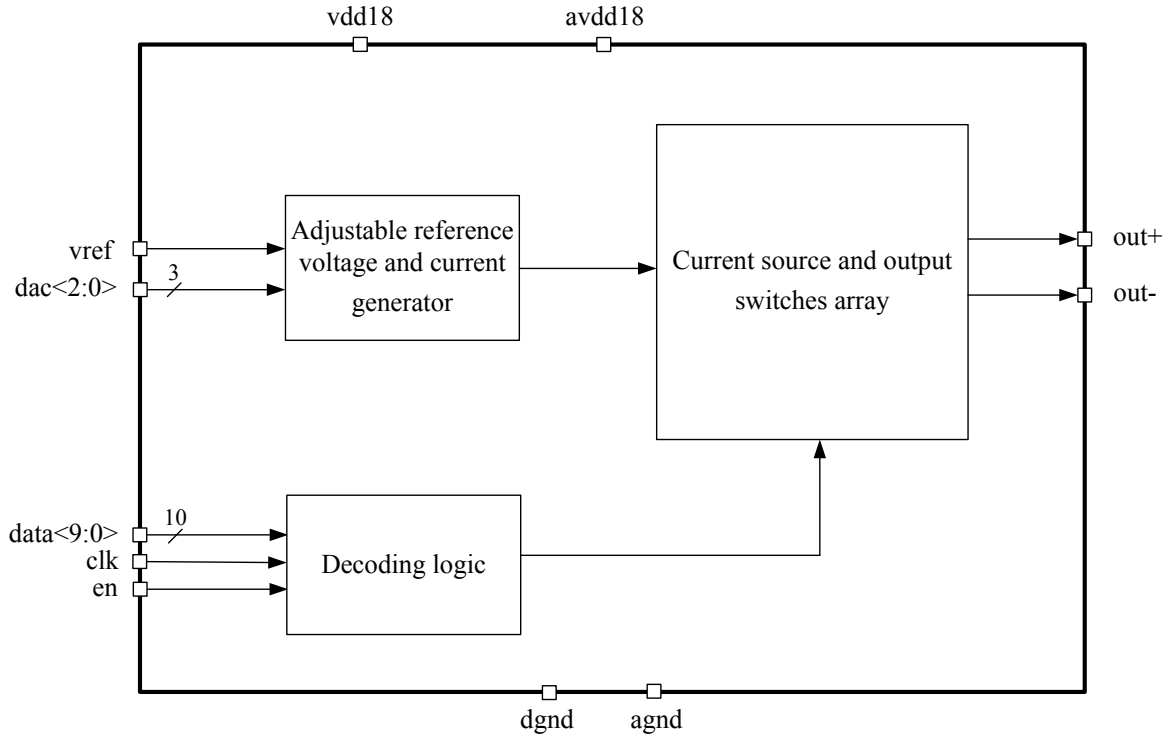

Figure 1: 10-bit DAC structure

5. PIN DISCRIPTION

Name	Direction	Description
en	I	Standby mode enable
clk	I	Clock input (100 MHz)
rst	I	Reset activation (the input is half of scale)
vref	I	Reference voltage input (1.2 V)
out+	O	Output differential signal
out-		
data<9:0>	I	Data input bus
dac <2:0>	I	Output current adjustment register
avdd18	I/O	Analog blocks supply voltage (1.8 V)
vdd18	I/O	Digital blocks supply voltage (1.8 V)
dgnd	I/O	Digital blocks ground
agnd	I/O	Analog blocks ground

6. LAYOUT DESCRIPTION

DAC layout dimensions are specified in table 1.

Table 1: DAC layout dimensions

Dimensions	Value	Unit
Height	665	um
Width	570	um

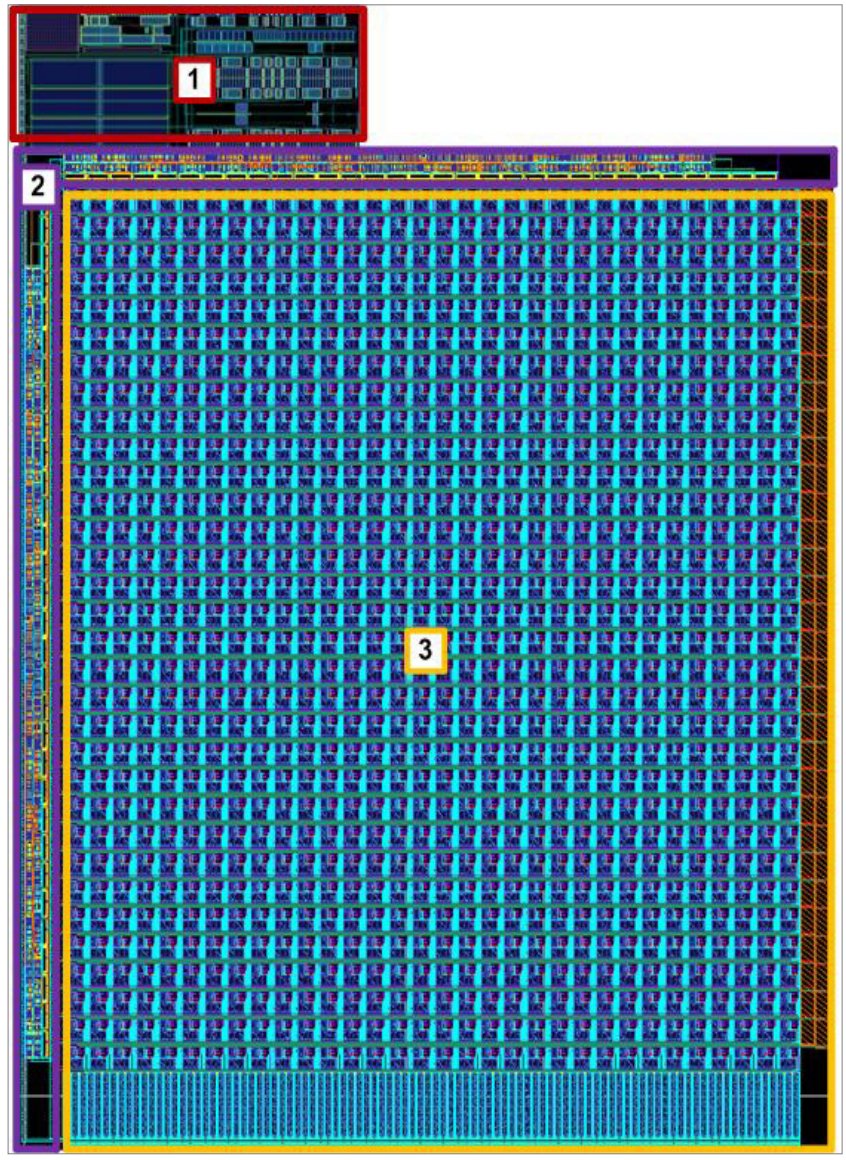

Figure 2: DAC layout

1. Adjustable reference voltage and current generator
2. Decoding logic
3. Current source and output switches array

7. OPERATIONAL CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology SMIC EEPROM CMOS 0.18 um
Status silicon proven
Area 0.38 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd18} = 1.7 ÷ 1.9 V, T_j = -60 ÷ +120 °C. Typical values are specified for V_{dd18} = 1.8 V, T_j = +27 °C.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Analog and digital blocks supply voltage	V_{dd18}	-	1.7	1.8	1.9	V
Operating temperature range	T_j	-	-60	27	+120	°C
Resolution	N	-	-	10	-	bits
Clock frequency	F_{clk}	-	-	100	-	MHz
Standby current	I_{st}	-	-	200	-	nA
Power consumption	P_{diss}	-	5.7	38	38	mW
Output current	I_{out}	-	1.3	-	21	mA
Spurious-free dynamic range	SFDR	Input frequency ≤ 25 MHz, load resistance 25 Ohm, F_{clk} = 100 MHz, output current register`s values set to dac<2:0> = “111”	60	62	66	dB
High input voltage level	V_{IH}	For digital inputs	1.3	-	-	V
Low input voltage level	V_{IL}		-	-	0.4	V

8. DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation