16-bit delta-sigma stereo, audio DAC

SPECIFICATION

1. FEATURES

- TSMC SiGe BiCMOS 0.18 um
- Resolution 16-bit
- 2-channel
- Different power supplies for digital and analog parts
- Sampling rates from 8 to 32 MHz
- Full power bandwidth up 25 kHz
- Standby mode (current consumption):
  1.2 nA analog parts
  0.05 uA digital parts
- Low-power dissipation:
  61.3 mW low impedance mode R_{load} = 32 Ohm
  5.95 mW low impedance mode R_{load} = 32 kOhm
- Spurious-free dynamic range:
  83 dB low impedance mode R_{load} = 32 Ohm
  76 dB high impedance mode R_{load} = 32 kOhm
- Signal-to-noise ratio:
  69 dB low impedance mode R_{load} = 32 Ohm
  73 dB high impedance mode R_{load} = 32 kOhm
- Small area 0.57 mm^2
- Portable to other technologies (upon request)

2. APPLICATION

- Portable devices

3. OVERVIEW

Delta-sigma stereo, audio DAC contains: reference voltage, control logic, digital buffers I2S interface (ws, sd, sck, gpio), two identical channels L and R: 2-order delta-sigma modulator, current steering DAC, low pass filter, analog buffer. Delta-sigma stereo, audio DAC requires 2.8 ÷3.6 V analog supply, 1.62 ÷ 1.98 V digital supply, reference current 4.95 ÷ 5.05 uA, input clock with duty cycle 45 ÷ 55 %. Delta-sigma stereo, audio DAC supports standby mode. There is the ability to configure the operating modes of the delta-sigma stereo, audio DAC with digital registers: register mode<2:0> controls the modes of the delta-sigma stereo, audio DAC and I2S interface (sd, ws), register mode_sck<2:0> controls the modes of I2S interface (sck), register mode_gpio<2:0> controls the modes of I2S interface (gpio). There is the ability to configure current consumption of the delta-sigma stereo, audio DAC with digital register: register adj_idc_buff<3:0> adjusts current of the analog buffer, register adj_idc_cs<3:0> adjusts current of the current steering DAC, register adj_idc_lpf<4:0> adjusts current of the low pass filter, signal enrc adjusts current of current steering DAC changing linearity of the current steering DAC.
Register adj_idc_cs<3:0> is also controls output voltage peak to peak.
The block is designed on TSMC SiGe BiCMOS 0.18 um technology.

4. STRUCTURE

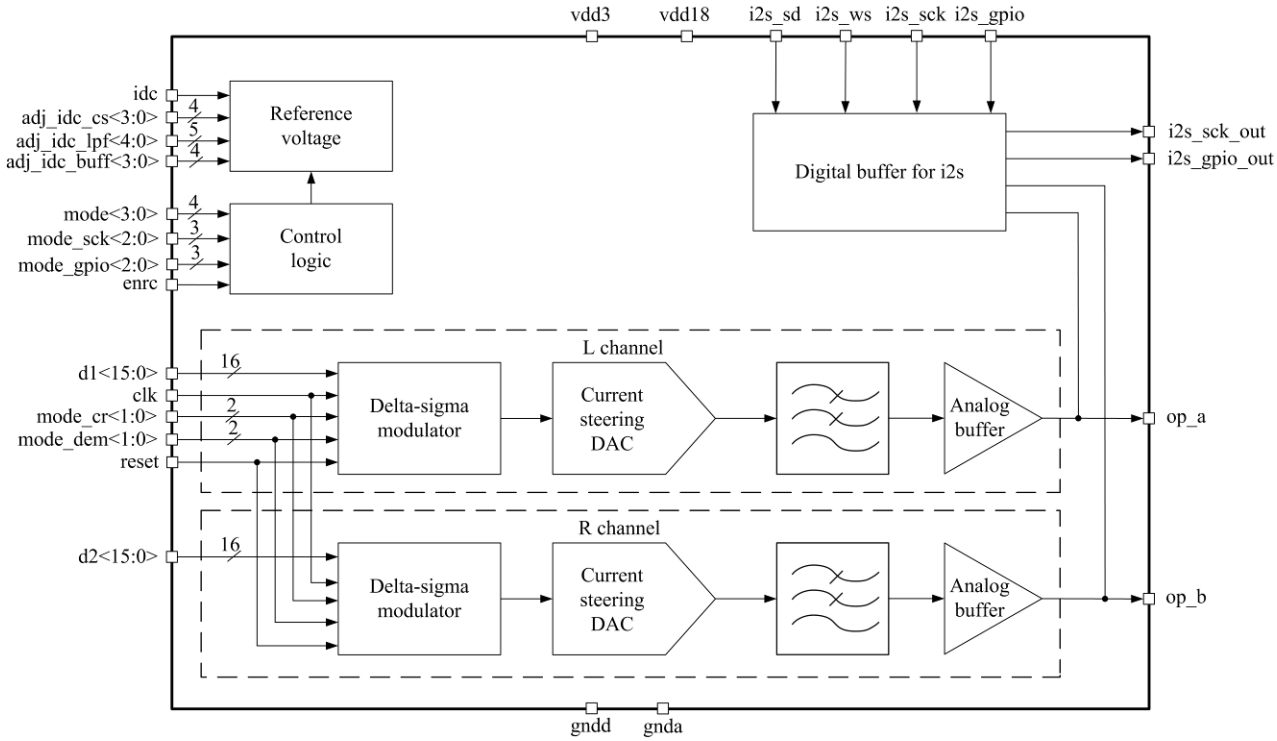

Figure 1: Structure delta-sigma stereo, audio DAC

5. PIN DISCRIPTION

Name	Direction	Description
idc	I	Reference current (5 uA)
i2s_sd	I	Input data I2S interface
i2s_ws	I	
i2s_sck	I	
i2s_gpio	I	
clk	I	Input clock
enrc	I	Signal of adjust modes the current steering DAC
reset	I	Signal of reset the delta-sigma modulator, active level – “1”
d1<15:0>	I	Input data line channel L
d2<15:0>	I	Input data line channel R
adj_idc_buff<3:0>	I	Register of adjust current the analog buffer
adj_idc_cs<3:0>	I	Register of adjust current the current steering DAC (output voltage range peak to peak)
adj_idc_lpf<4:0>	I	Register of adjust current the low pass filter
mode<3:0>	I	Register of adjust modes the delta-sigma DAC and the I2S interface (sd, ws)
mode_sck<2:0>	I	Register of adjust modes the I2S interface (sck)
mode_gpio<2:0>	I	Register of adjust modes the I2S interface (gpio)
mode_cr<1:0>	I	Register of adjust modes of correction the delta-sigma modulator
mode_dem<1:0>	I	Register of adjust frequency of dem correction
op_a	O	Output signal channel L
op_b	O	Output signal channel R
i2s_sck_out	O	Output data line I2S interface
i2s_gpio_out	O	
vdd18	I/O	Digital block supply voltage (1.8 V)
vdd3	I/O	Analog block supply voltage (3 V)
gndd	I/O	Digital blocks ground
gnda	I/O	Analog blocks ground

6. LAYOUT DESCRIPTION

Delta-sigma stereo, audio layout dimensions are given in the table 1.

Table 1: Block dimension

Dimension	Value	Unit
Height	500	um
Width	1120	um

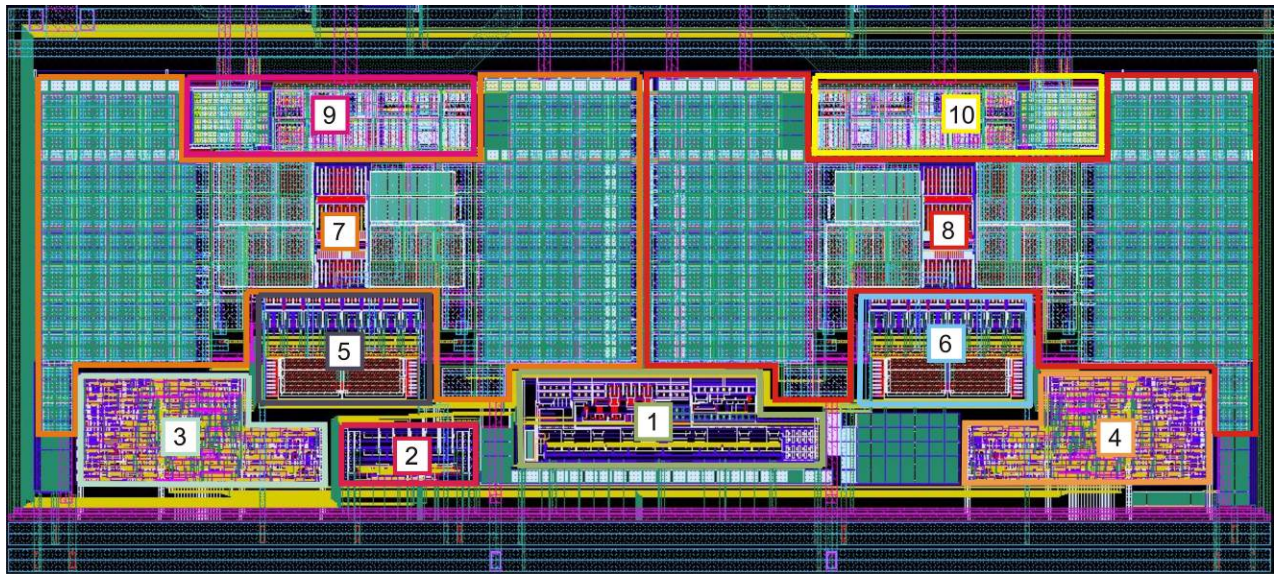

Figure 2: Layout delta-sigma stereo, audio DAC

1. Reference voltage
2. Control logic
3, 4. Delta-sigma modulator (L and R channels)
5, 6. Current steering DAC (L and R channels)
7, 8. Low pass filter (L and R channels)
9, 10. Analog buffer (L and R channels)

Digital buffer I2S interface dimensions are given in the table 2.

Table 2: Block dimension

Dimension	Value	Unit
Height	104	um
Width	53	um

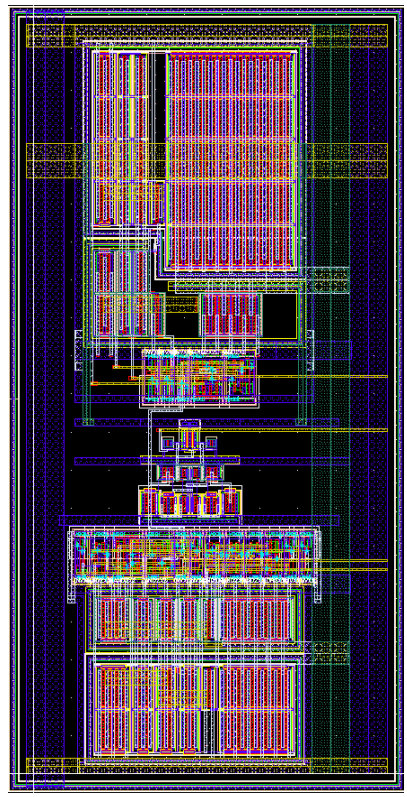

Figure 3: Layout digital buffer I2S interface

7. OPERATIONAL CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC SiGe BiCMOS 0.18 um
Status silicon proven
Area 0.57 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dda} = 2.8÷3.6 V, V_{ddd}=1.62÷1.98 V and T_j =-40÷80 °C, typical values are at V_{dda} = 3.0 V, V_{ddd}=1.8 V, T_j = 27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Analog blocks supply voltage	V_{dda}	-	2.8	3.0	3.6	V
Digital blocks supply voltage	V_{ddd}	-	1.62	1.8	1.98	V
Operating temperature range	T_j	-	-40	27	+80	°C
Reference current	I_{ref}	-	4.95	5.00	5.05	uA
Duty cycle	S	-	45	50	55	%
Resolution	N	-	-	16	-	bit
Clock frequency	F_{clk}	-	8	-	32	MHz
Oversampling ratio	OSR	-	-	512	-	-
Standby current	I_s	Analog parts	1.0	1.2	8.9	nA
		Digital parts	0.008	0.05	5.4	uA
Output voltage range peak to peak	$A_{IN\ p\text{-}p}$	-	-	1	-	V
Full power bandwidth	F_b	-	-	25	-	kHz
Current consumption digital parts	I_{cn}	F_{clk} = 25 MHz F_b = 12.2 kHz mode<2:0> = “010” mode_sck<1:0> = “00” adj_idc_cs<3:0> = “1011” adj_idc_lpf<4:0> = “01010” adj_idc_buf<3:0> = “1010” enrc = “1”	-	0.5	-	mA

Table “electrical characteristics” (continue)

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Current consumption analog parts	I_{cn}	F_{clk} = 25 MHz F_b = 12.2 kHz R_{load} = 32 Ohm mode<2:0> = “010” mode_sck<1:0> = “00” adj_idc_cs<3:0> = “1011” adj_idc_lpf<4:0> = “01010” adj_idc_buf<3:0> = “1010” enrc = “1”	-	20	-	mA
		F_{clk} = 25 MHz F_b = 12.2 kHz without R_{load} mode<2:0> = “010” mode_sck<1:0> = “00” adj_idc_cs<3:0> = “1011” adj_idc_lpf<4:0> = “01010” adj_idc_buf<3:0> = “1010” enrc = “1”	11.8	13	16.22	mA
		F_{clk} = 25 MHz F_b = 12.2 kHz R_{load} = 32 kOhm mode<2:0> = “001” mode_sck<1:0> = “00” adj_idc_cs<3:0> = “1011” adj_idc_lpf<4:0> = “11111” adj_idc_buf<3:0> = “1010” enrc = “1”	1.52	1.55	1.63	mA
Spurious-free dynamic range	SFDR	F_{clk} = 25 MHz F_b = 12.2 kHz R_{load} = 32 Ohm mode<2:0> = “010” mode_sck<1:0> = “00” adj_idc_cs<3:0> = “1011” adj_idc_lpf<4:0> = “01010” adj_idc_buf<3:0> = “1010” enrc = “1”	-	83	-	dB
		F_{clk} = 25 MHz F_b = 12.2 kHz R_{load} = 32 kOhm mode<2:0> = “001” mode_sck<1:0>= “00” adj_idc_cs<3:0> = “1011” adj_idc_lpf<4:0>= “11111” adj_idc_buf<3:0>= “1010” enrc = “1”	-	76	-	dB

Table “electrical characteristics” (continue)

Parameter	Symbol	Condition	Value			
			min	typ.	max	
Signal-to-noise ratio	SNR	F_{clk} = 25 MHz F_b = 12.2 kHz R_{load} = 32 Ohm mode<2:0> = “010” mode_sck<1:0> = “00” adj_idc_cs<3:0> = “1011” adj_idc_lpf<4:0> = “01010” adj_idc_buf<3:0> = “1010” enrc = “1”	-	69	-	dB
		F_{clk} = 25 MHz F_b = 12.2 kHz R_{load} = 32 kOhm mode<2:0> = “001” mode_sck<1:0>= “00” adj_idc_cs<3:0> = “1011” adj_idc_lpf<4:0> = “11111” adj_idc_buf<3:0> = “1010” enrc = “1”	-	73	-	dB
Clock frequency I2S interface	F_{clk}	C_{load} = 10 pF	-	-	32	MHz
High input voltage level	V_{IH}	-	$0.7V_{ddd}$	-	-	V
Low input voltage level	V_{IL}		-	-	$0.3V_{ddd}$	V

8. TYPICAL CHARACTERISTICS

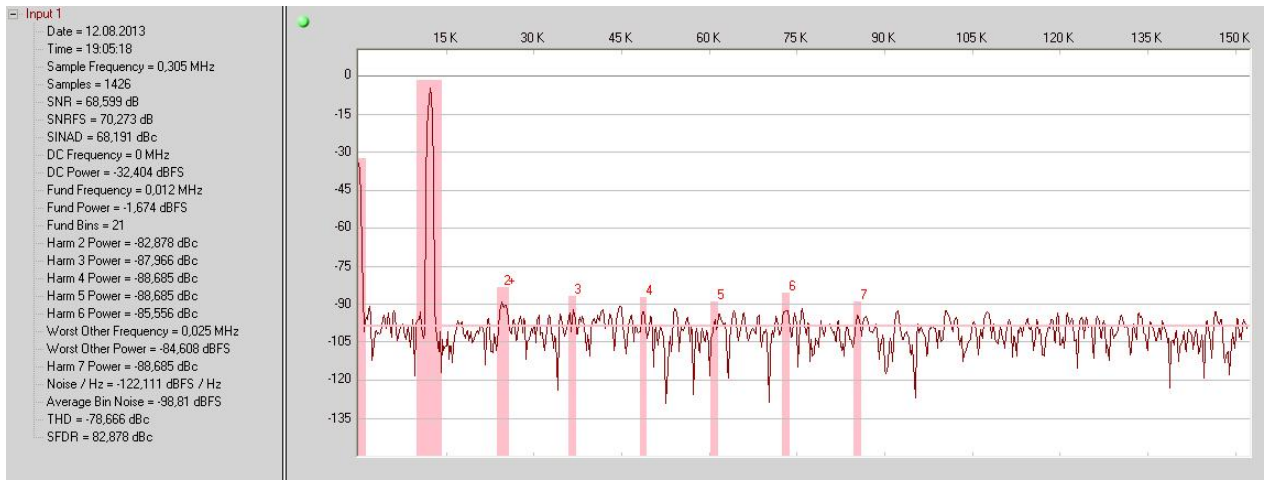

Figure 4: Spectrum, low impedance load (mode<2:0> = “010”), R_{load} = 32 Ohm

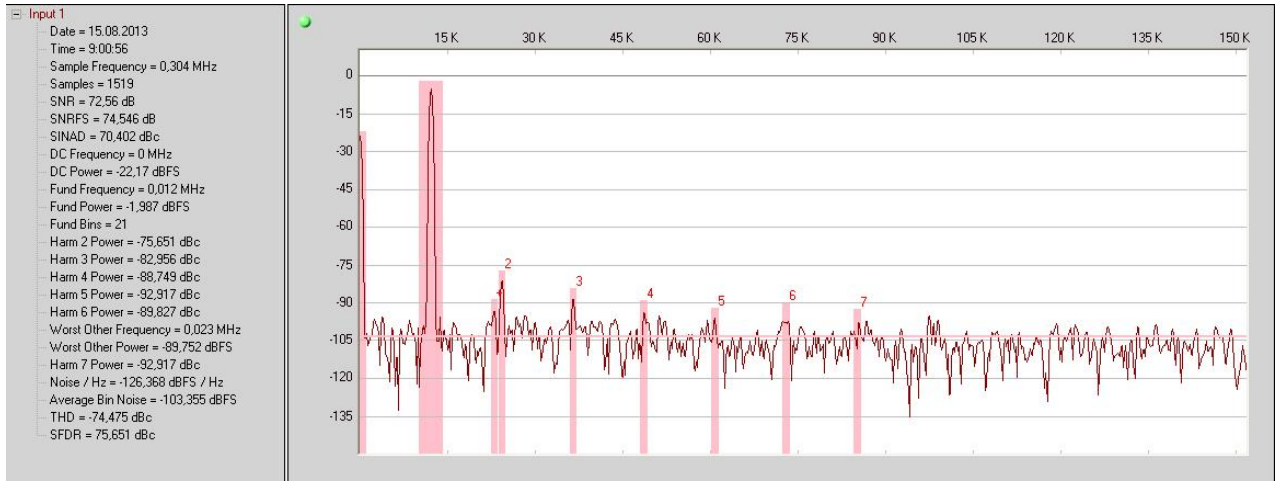

Figure 5: Spectrum, high impedance load (mode<2:0> = “010”), R_{load} = 32 kOhm

9. DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

1. From version 1.1:
   - Section 1 was changed (refer to page 1)
   - Subsection 7.1 was changed (refer to page 6)