12-bit 2-channel 50 MSPS current steering DAC

SPECIFICATION

1 FEATURES

- TSMC CMOS 180 nm
- Resolution 12 bit
- 2-channel
- Different power supplies for digital (3.3 V) and analog parts (3.3 V)
- Sampling rate up to 50 MSPS
- Standby mode (current consumption 100 nA)
- Power dissipation:
  75.24 mW at 50 MSPS and 10 mA full scale output current
- Differential current output range from 5 mA to 20 mA
- Spurious-free dynamic range:
  88 dB at 50 MSPS and fin = 1.575 MHz and 10 mA output current
  89 dB at 50 MSPS and fin = 11.513 MHz and 10 mA output current
- Signal-to-noise ratio:
  70 dB at 50 MSPS and fin = 1.575 MHz and 10 mA output current
  70 dB at 50 MSPS and fin = 11.513 MHz and 10 mA output current
- Signal-to-noise and distortion ratio:
  70 dB at 50 MSPS and fin = 1.575 MHz and 10 mA output current
  70 dB at 50 MSPS and fin = 11.513 MHz and 10 mA output current
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Wireless infrastructures
- Broadband communications
- Picocell, femtocell base stations
- Medical instrumentation
- Ultrasound transducer excitation
- Signals and arbitrary waveform generators

3 OVERVIEW

12-bit 50 MSPS dual current steering DAC contains two DAC cores, reference current, bandgap, configuration register. Core DAC is based on current steering architecture and contains control logic, current source, switches array and reference voltage. There are two operation modes: with external reference current and internal reference current, which independent from voltage supply, temperature and dependent from process variations of resistor. DAC has a feature of adjusting output current. A segmented DAC architecture and Q^2 random walk algorithm are used. DAC requires: 3.0 ÷ 3.6 V analog supply, 3.0 ÷ 3.6 V digital supply, differential input clock signal with duty cycle 45 ÷ 55%. 12-bit 50 MSPS dual current steering DAC supports standby mode.
The block is designed on TSMC CMOS 180 nm technology.

4 STRUCTURE

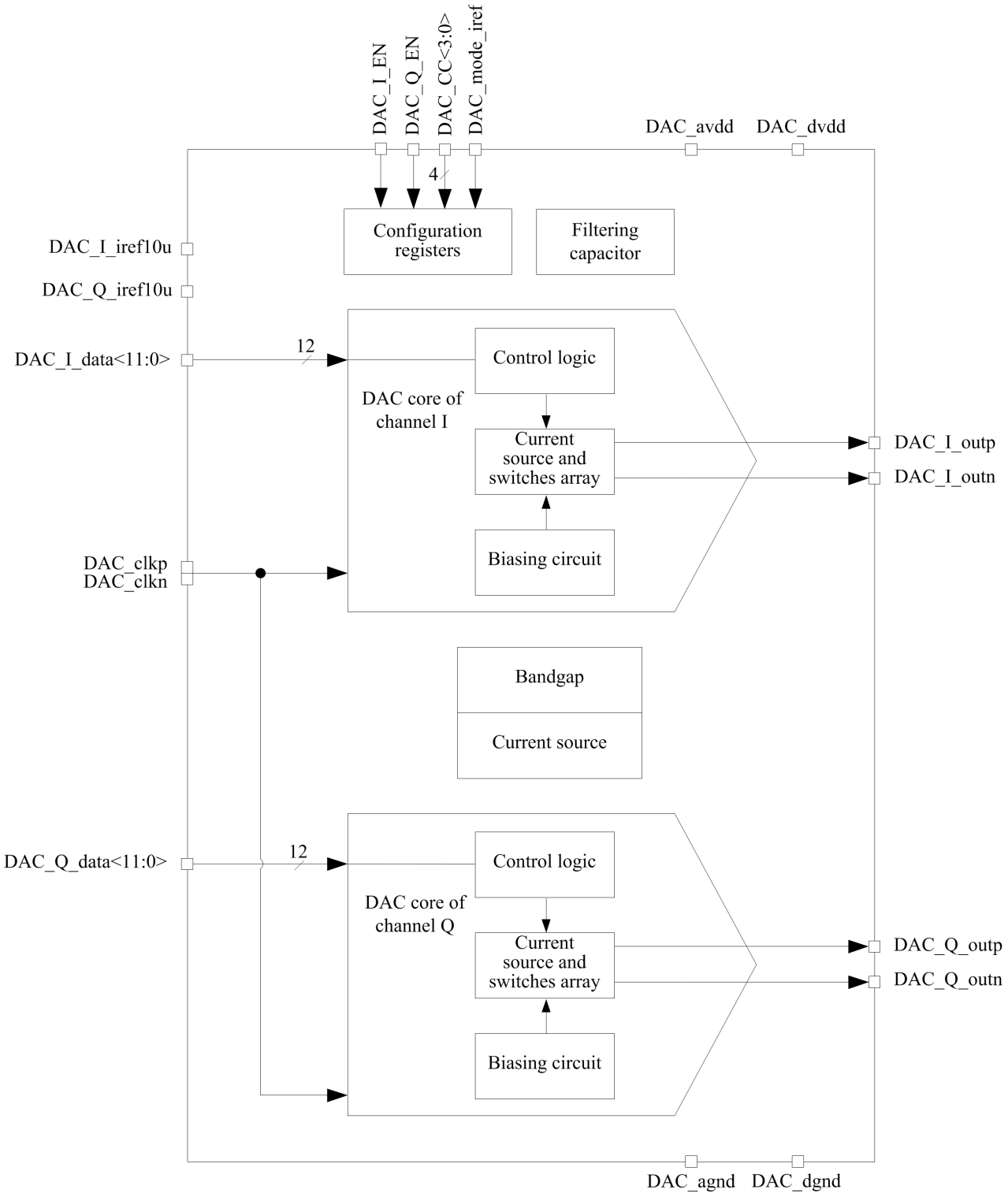

Figure 1: 12-bit 50 MSPS dual current steering DAC structure

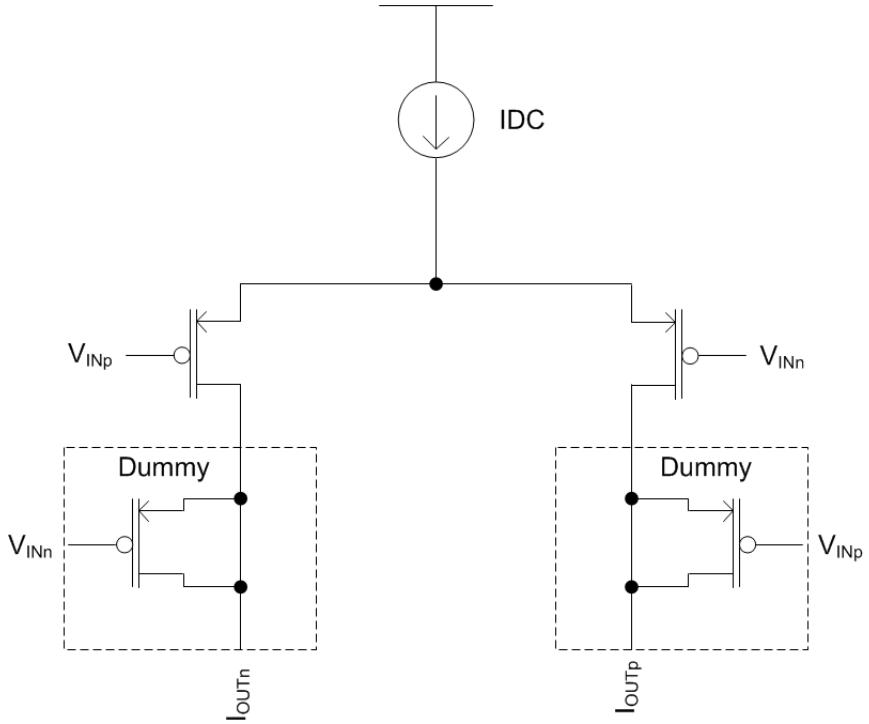

Figure 2: Current cell simplified view

5 PIN DESCRIPTION

Name	Direction	Description
DAC_I_iref10u	I	Reference current of channel I (10 uA)
DAC_Q_iref10u	I	Reference current of channel Q (10 uA)
DAC_clkp DAC_clkn	I	Differential input clock
DAC_I_EN	I	Enable of channel I
DAC_Q_EN	I	Enable of channel Q
DAC_mode_iref	I	Enable of external reference current
DAC_I_data<11:0>	I	Data input of channel I
DAC_Q_data<11:0>	I	Data input of channel Q
DAC_CC<3:0>	I	Register of adjustment output current range
DAC_I_outp DAC_I_outn	O	Differential output current of channel I
DAC_Q_outp DAC_Q_outn	O	Differential output current of channel Q
DAC_avdd	I/O	Analog blocks supply voltage (3.3 V)
DAC_dvdd	I/O	Digital blocks supply voltage (3.3 V)
DAC_agnd	I/O	Analog blocks ground
DAC_dgnd	I/O	Digital blocks ground

6 LAYOUT DESRIPTION

12-bit 50 MSPS dual current steering DAC layout dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	915	um
Width	743	um

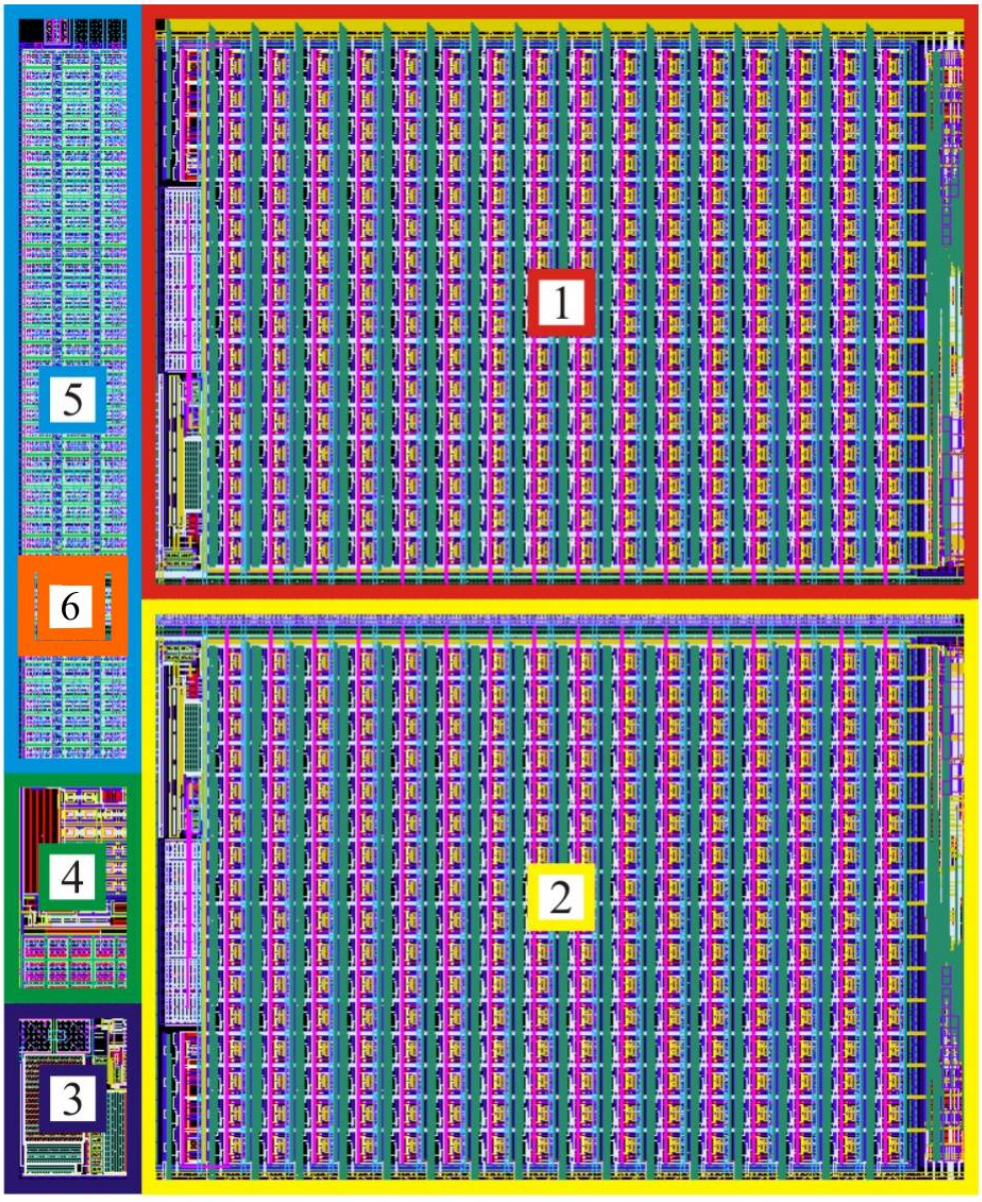

Figure 3: 12-bit 50 MSPS dual current steering DAC layout

1. DAC core of channel Q
2. DAC core of channel I
3. Reference current
4. Bandgap
5. Filtering capacitor
6. Configuration register

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS 180 nm
Status silicon proven
Area 0.68 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd_a} = 3.0÷3.6 V, V_{dd_d} = 3.0÷3.6 V and T_j =-40 ÷ +125 °C, typical values are at V_{dd_a} = 3.3 V, V_{dd_d} = 3.3 V and T_j = 27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Analog blocks supply voltage	V_{dd_a}	-	3.0	3.3	3.6	V
Digital blocks supply voltage	V_{dd_d}	-	3.0	3.3	3.6	V
Operating temperature range	T_j	-	-40	27	+125	°C
Reference current	I_{ref}	-	9.8	10	10.2	uA
Output current range	$I_{OUT\ p\text{-}p}$	DAC_CC<3:0> = “0000”	-	5	-	mA
		DAC_CC<3:0> = “0101”	-	10	-	mA
		DAC_CC<3:0> = “1111”	-	20	-	mA
Resolution	N	-	-	12	-	bit
Duty cycle	S	-	45	50	55	%
Sampling rate	F_s	-	0	-	50	MSPS
Standby current	I_S	-	-	100	-	nA
Power dissipation	P_{cn}	DAC_CC<3:0> = “0101”	-	75.24	-	mW
Current consumption	I_{cn}	DAC_CC<3:0> = “0101”	-	22.8	-	mA
Input high-logic level	V_{IH}	-	$0.7V_{dd\_d}$	-	-	V
Input low-logic level	V_{IL}	-	-	-	$0.3V_{dd\_d}$	V

7.3 DYNAMICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{dd_a} = 3.0÷3.6 V, V_{dd_d} = 3.0÷3.6 V and T_j =-40 ÷ +125 °C, typical values are at V_{dd_a} = 3.3 V, V_{dd_d} = 3.3 V and T_j = 27° C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Spurious-free dynamic range	SFDR	DAC_CC<3:0> = “0101” F_{in} = 1.575 MHz	-	88	-	dB
		DAC_CC<3:0> = “0101” F_{in} = 11.513 MHz	-	89	-	dB
Signal-to-noise ratio	SNR	DAC_CC<3:0> = “0101” F_{in} = 1.575 MHz	-	70	-	dB
		DAC_CC<3:0> = “0101” F_{in} = 11.513 MHz	-	70	-	dB
Signal-to-noise and distortion ratio	SINAD	DAC_CC<3:0> = “0101” F_{in} = 1.575 MHz	-	70	-	dB
		DAC_CC<3:0> = “0101” F_{in} = 11.513 MHz	-	70	-	dB

8 TYPICAL CHARACTERISTICS

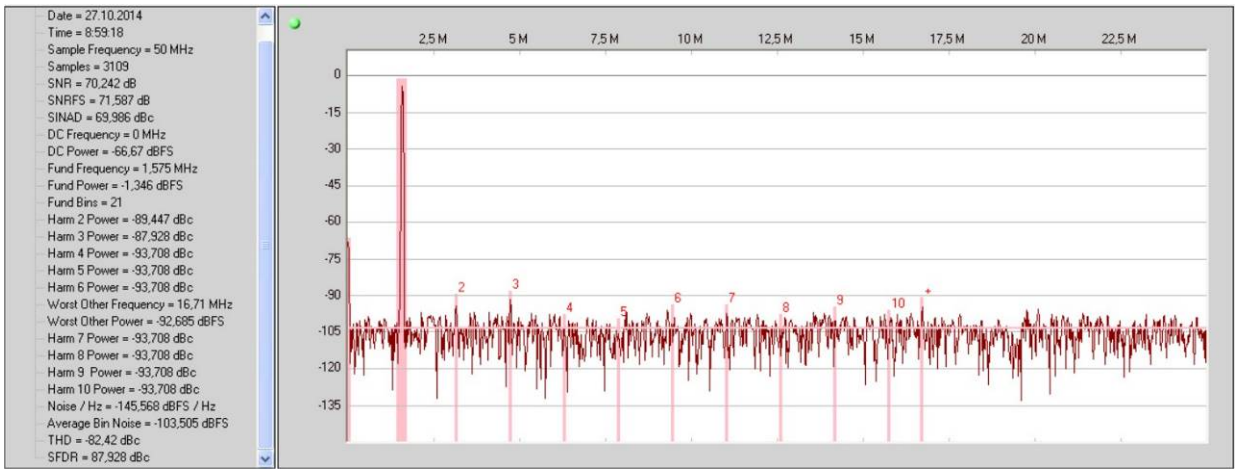

Figure 4: Spectrum, F_s= 50 MSPS, F_{in}= 1.575 MHz

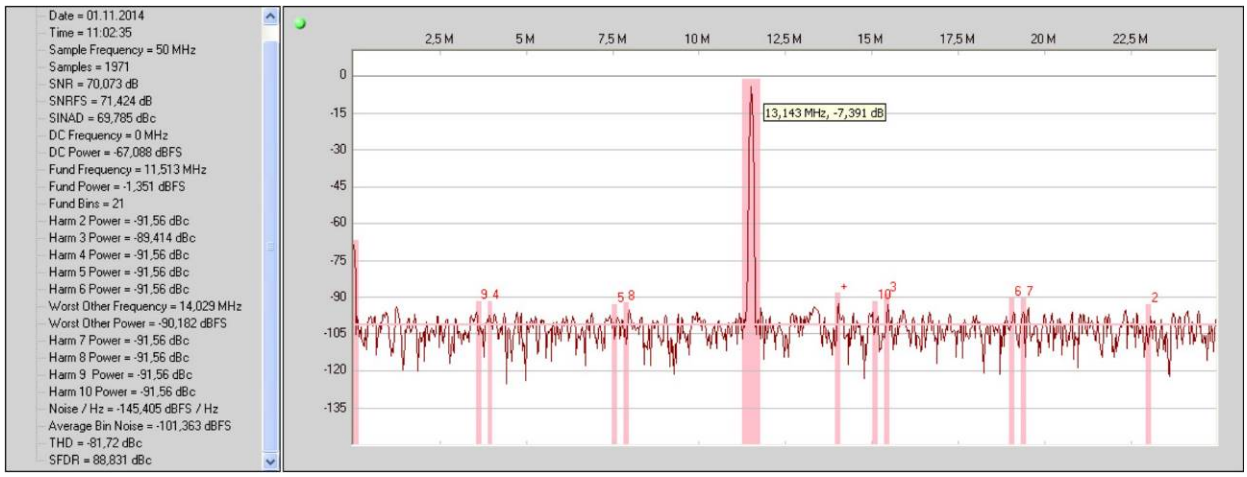

Figure 5: Spectrum, F_s= 50 MSPS, F_{in}= 11.513 MHz

9 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.0:

- Section 1 was changed (refer to page 1)
- Section 6 was changed (refer to page 5)
- Subection 7.1 was changed (refer to page 6)
- Subection 7.2 was changed (refer to page 6)
- Subection 7.3 was changed (refer to page 6)