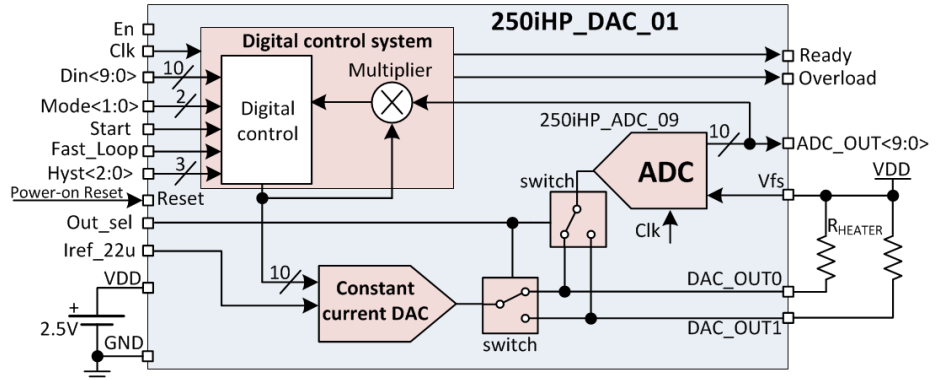


10-bit 1-channel constant power DAC

OVERVIEW

10-bit Constant power DAC employs a current steering DAC architecture with control loop, which adjusts DAC input code to keep power dissipated in terminator constant. The block is easy to configure and operate, combining good accuracy and linearity. Several operation modes are available: constant power DAC, current DAC with output voltage monitoring, current DAC (manual mode), low-speed ADC. Output DAC current could be fed to one of two DAC outputs (DAC_OUT0 or DAC_OUT1) depending on Out_sel input.



IP technology: iHP sg25H4.

IP status: pre-silicon verification.

Layout dimensions: 0.508x0.572mm. Total area: 0.28 mm².

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
Supply voltage	V _{DD}	-	2.375	2.50	2.625	V
Operating temperature range	T _J	-	0	50	100	°C
DAC Resolution	N _{DAC}	-	-	10	-	bit
ADC Resolution	N _{ADC}	-	-	10	-	bit
Input reference current	I _{REF}	-	-	20	-	uA
Full-scale output current	I _{OUT}	Mode = "01", Mode = "10"	-	22	-	mA
Full-scale output power	P _{OUT}	Mode = "11"	-	-	56.3	mW
Power adjustment step	P _{step}	Mode = "11" R _{HEATER} =120 Ohm	55	-	-	uW
CDAC Differential nonlinearity	DNL	V _{DAC_OUT} > 0.3 V	-	0.6	-	LSB
CDAC Integral nonlinearity	INL	V _{DAC_OUT} > 0.3 V	-	< 1	-	LSB
Output resistance	R _{OUT}	1 LSB current	-	100	-	kOhm
Targeted load resistance	R _{LOAD}	-	-	125	-	Ohm
Clock frequency	F _{CLK}	-	-	32	-	kHz
Clock Input Duty Cycle	S	-	45	50	55	%
Clock Signal Period Jitter	T _{JIT}	-	-	-	50	nS
Full-Scale ADC voltage	V _{FS}	-	-	2.5	V _{DD}	V
Current consumption	I _{DD} *	Mode = "00"	-	-	0.002	mA
		Mode = "01"	0.05	0.10	0.15	
		Mode = "10"	0.05	0.10	0.15	
		Mode = "11"	0.05	0.10	0.20	
	I _{STB}	Standby mode	15	100	500	nA
Input logic high level	V _{IH}	For digital inputs	V _{DD} -0.25	-	V _{DD} +0.25	V
Input logic low level	V _{IL}		-0.25	-	0.25	V

* - excluding load current and VFS current consumption