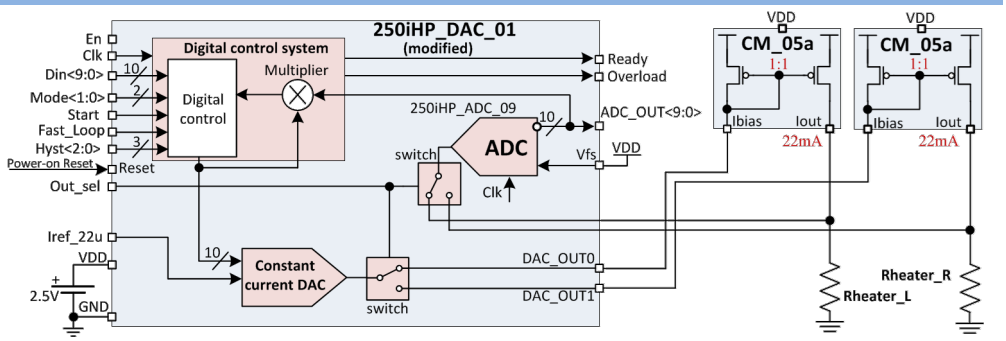
10-bit Constant Power DAC

OVERVIEW



10-bit constant power DAC employs a current steering DAC architecture with control loop, which adjusts DAC input code to keep power dissipated in terminator constant. The block is easy to configure and operate, combining good accuracy and linearity. Several operation modes are available: constant power DAC, current DAC with output voltage monitoring, current DAC (manual mode), low-speed ADC. Output DAC current could be fed to one of two DAC outputs (DAC_OUT0 or DAC_OUT1) depending on Out_sel input. IP 250iHP_DAC_02 is modified version of previously designed Constant power DAC - 250iHP_DAC_01. Design modification was targeting change of output current polarity. In order to do this, following changes were made: pmos-type current mirrors 250iHP_CM_05a were added at outputs DAC_OUT0, DAC_OUT1; ADC inputs are separate pins now to probe voltage at outputs of 250iHP_CM_05a cells; ADC output is inverted to deal with changed output current and voltage polarity.

IP technology: iHP SiGe BiCMOS 0.25um.

IP status: silicon proven.

Area: PDAC unit (250iHP_DAC_01) - 0.28 mm^2; current mirror units (250iHP_CM_05a) - 0.12 mm^2

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
Supply voltage	V_{DD}	-	2.375	2.50	2.625	V
Operating temperature range	T_J	-	0	50	100	ºC
DAC Resolution	N_{DAC}	-	-	10	-	bit
ADC Resolution	N_{ADC}		-	10	-	bit
Input reference current	I_{REF}	-	-	20	-	uA
Full-scale output current	I_{OUT}	Mode = “01”, Mode = “10”	-	22	-	mA
Full-scale output power	P_{OUT}	Mode = “11”	-	-	56.3	mW
Power adjustment step	Pstep	Mode = “11” RHEATER = 120 Ohm	55	-	-	uW
CDAC Differential nonlinearity	DNL	VDAC_OUT > 0.3 V	-	0.6	-	LSB
CDAC Integral nonlinearity	INL	VDAC_OUT > 0.3 V	-	< 1	-	LSB
Output resistance	R_{OUT}	1 LSB current	-	100	-	kOhm
Targeted load resistance	R_{LOAD}	-	-	125	-	Ohm
Clock frequency	F_{CLK}	-	-	32	-	kHz
Clock Input Duty Cycle	S	-	45	50	55	%
Clock Signal Period Jitter	T_{JIT}	-	-	-	50	nS
Full-Scale ADC voltage	V_{FS}	-	-	2.5	VDD	V
Current consumption	I_{DD}*	Mode = “00”	-	-	0.002	mA
		Mode = “01”	0.05	0.10	0.15	
		Mode = “10”	0.05	0.10	0.15	
		Mode = “11”	0.05	0.10	0.20	
	I_{STB}	Standby mode	15	100	500	nA
Input logic high level	V_{IH}	For digital inputs	VDD-0.25	-	VDD+0.25	V
Input logic low level	V_{IL}		-0.25	-	0.25	V

* - excluding load current and VFS current consumption