

# 5-bit programmable ECL high-frequency divider

## SPECIFICATION

### 1 FEATURES

- AMS035 BiCMOS 0.35  $\mu\text{m}$
- Differential structure
- Dividing ratio is regulated in the range of 16 ...62 with step 2
- Input differential signal frequency up to 1.7 GHz
- Input signal duty cycle is 0.5
- Scalable structure
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra, X-FAB

### 2 APPLICATION

- PLL frequency synthesizer

### 3 OVERVIEW

The 5-bit programmable ECL high-frequency divider is a set of serially connected dividers with the varied dividing ratio  $2/3$  that is able to scale the structure either into minimum dividing ratio decreasing or maximum dividing ratio increasing. The differential circuit has higher noise immunity. An output divider  $/2$  based on D-trigger provides an input signal duty cycle of 0.5. The block is fabricated on AMS BiCMOS 0.35  $\mu\text{m}$  technology.

### 4 STRUCTURE

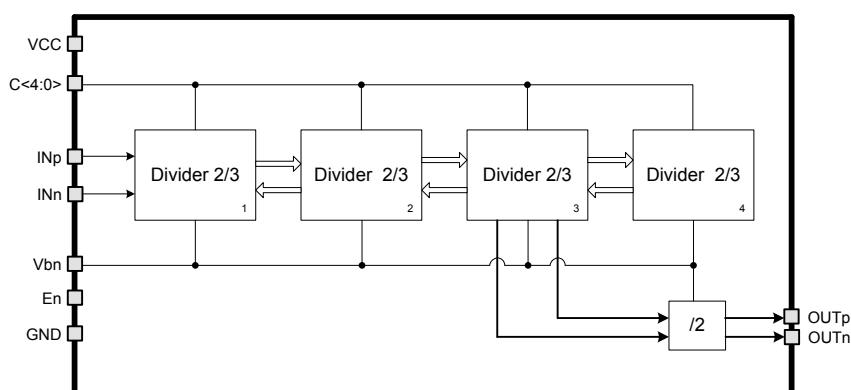


Figure 1: 5-bit programmable ECL high-frequency divider structure

## 5 PIN DESCRIPTION

Name	Direction	Description
INp	I	Analog differential input
INn	I	
C<4:0>	I	Digital code of dividing ratio
Vbn	I	Reference voltage of current source
En	I	Enable/disable of divider
OUTp	O	Analog differential output
OUTn	O	
VCC	IO	Supply voltage
GND	IO	Ground

## 6 LAYOUT DESCRIPTION

5-bit programmable ECL high-frequency divider dimensions are given in the table 1.

**Table 1:** Block dimensions

Dimension	Value	Unit
Height	214	$\mu\text{m}$
Width	485	$\mu\text{m}$

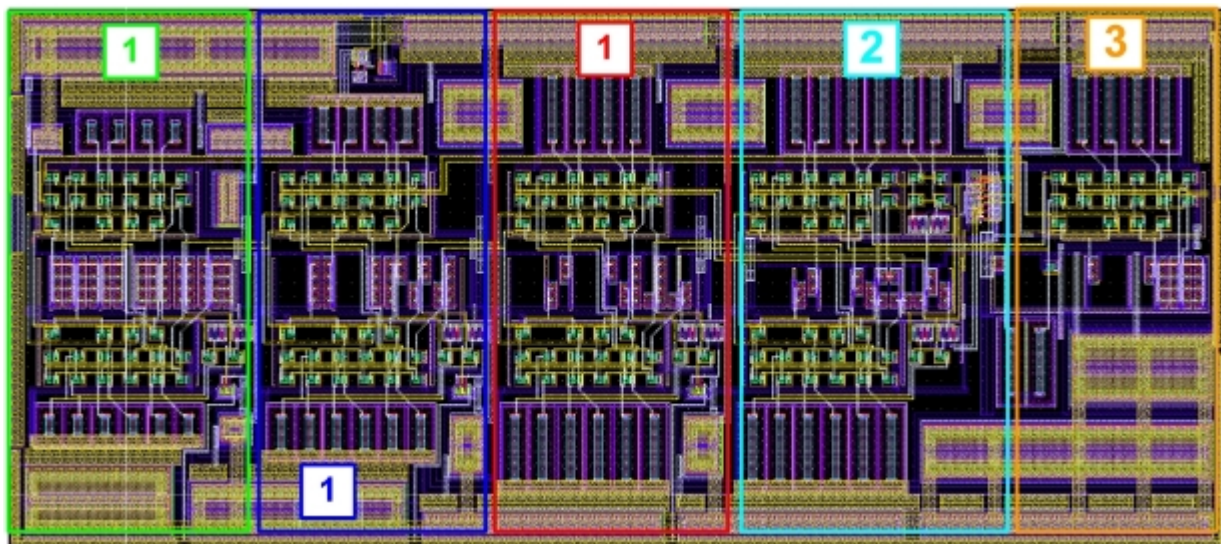


Figure 2: Block layout

1. Frequency divider 2/3
2. Frequency divider 2/3 with control logic
3. Input divider /2

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ AMS BiCMOS 0.35  $\mu\text{m}$   
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_ 0.104  $\text{mm}^2$

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc} = 2.4 \div 3.6 \text{ V}$  and  $T_j = -40 \div +85^\circ\text{C}$ . Typical values are at  $V_{cc} = 2.7 \text{ V}$ ,  $T_j = +27^\circ\text{C}$ , unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	$V_{cc}$	-	2.4	2.7	3.6	V
Operating temperature range	$T_j$	-	-40	27	85	$^\circ\text{C}$
Dividing ratio	C	-	16	-	62	-
Input frequency	$F_{IN}$	-	-	-	1.7	GHz
Peak-to-peak input voltage	$A_{in\_p-p}$	At differential input	0.3	0.4	0.8	V
In-phase component of input signal	$A_{in\_dc}$	$V_{cc}=2.7 \text{ V}$	1.5	1.7	2	V
Peak-to-peak output voltage	$A_{out\_p-p}$	At differential input	0.3	0.4	0.55	V
In-phase component of output signal	$A_{out\_dc}$	$V_{cc}=2.7 \text{ V}$	1.6	1.8	2	V
Supply current	$I_{dd}$	-	-	1.5	-	mA
Stand-by current	$I_{st}$	-	-	15	100	nA
Input logic-level high	$V_{IH}$	-	$0.9V_{cc}$	-	$V_{cc}$	V
Input logic-level low	$V_{IL}$	-	-0.2	0	0.2	V

## 8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation