Programmable 6-bit CMOS frequency divider

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Range of division ratio from 1 to 63
- Division ratio change with step 0.5
- Compact structure
- Portable to other technologies (upon request)

2 APPLICATION

- PLL frequency synthesizer

3 OVERVIEW

The programmable 6-bit CMOS frequency divider is a set of two independent circuits. One of them is designed using 6-bit counter and is able to change input frequency division ratio with step 1. The second part is based on a set of serially connected dividers with the varied division ratio 2/3 and is able to change division ratio with step 0.5. Since this structure consists of the static triggers, current consumption is closed to zero when there is no input clock. The division ratio is defined by the digital code RDIV_R<5:0>. RFAC bit is a fractional part of division ratio.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

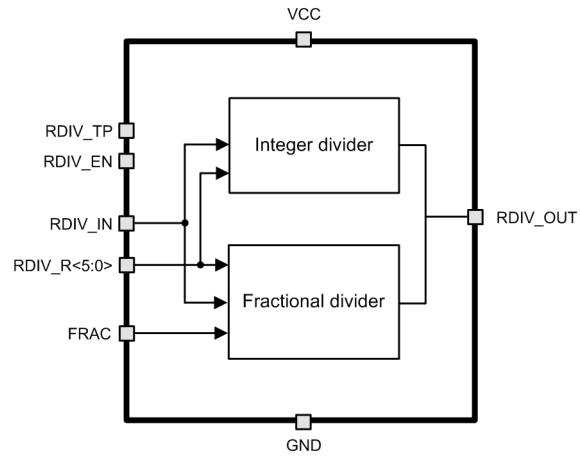

Figure 1: Programmable 6-bit CMOS frequency divider structure

5 PIN DESCRIPTION

Name	Direction	Description
RDIV_IN	I	Divider input
RDIV_R<5:0>	I	Digital code of division ratio
RDIV_TP	I	Type selection: integer/fractional
FRAC	I	Division ratio fractional part
RDIV_EN	I	Enable/disable of divider
RDIV_OUT	O	Divider output
VCC	IO	Supply voltage
GND	IO	Ground

6 LAYOUT DESCRIPTION

Programmable 6-bit CMOS frequency divider dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	106	um
Width	83	um

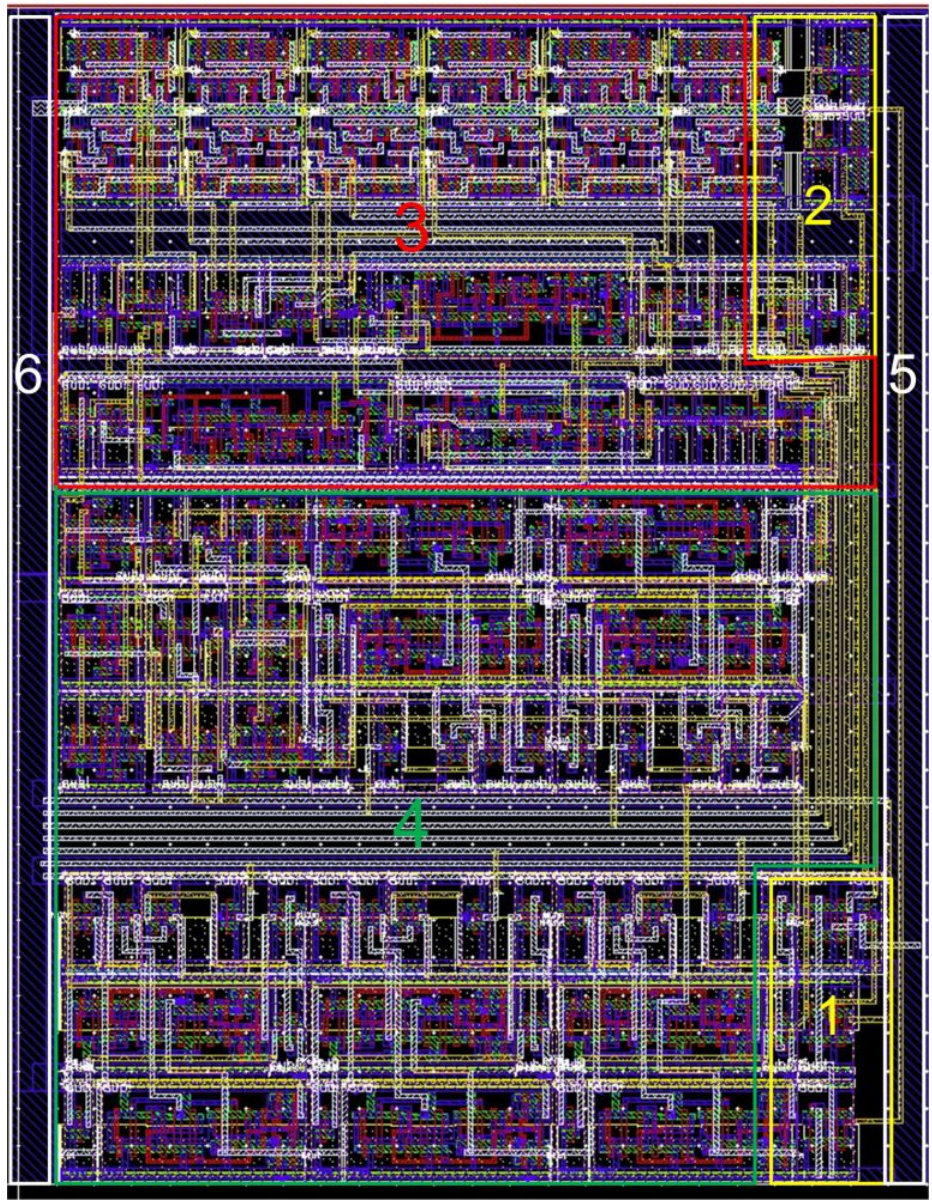

Figure 2: Frequency divider layout

1. Control logic
2. Output buffer
3. Integer divider
4. Fractional divider
5. Supply voltage bus
6. Ground bus

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
Status _____ silicon proven
Area _____ 0.008 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{cc} = 1.8 \div 2.7$ V and $T_j = -60 \div +125$°C. Typical values are at $V_{cc} = 2.0$ V, $T_j = +27$°C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.8	2	2.7	V
Operating temperature range	T_j	-	-60	27	+125	°C
Division ratio	R	-	1	-	63	-
Input frequency	F_{IN}	-	-	10	300	MHz
Peak-to-peak input voltage	A_{in_in}	-	1.8	2	2.7	V
Peak-to-peak output voltage	$A_{out\_p\text{-}p}$	-	1.8	2	2.7	V
Supply current	I_{dd}	F_{IN} = 10 MHz	-	14	-	uA
Stand-by current	I_{st}	-	-	0.6	-	nA
Input logic-level high	V_{IH}	For digital inputs	$0.9V_{cc}$	-	$1.1V_{cc}$	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation