# Programmable CMOS PLL high-frequency divider

# SPECIFICATION

## 1 FEATURES

- TSMC BiCMOS 0.18 um
- Wide range of dividing ratio 16…1023
- Low current consumption
- Compact structure
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

## 2 APPLICATION

- PLL frequency synthesizer

## 3 OVERVIEW

The CMOS PLL high-frequency divider consists of the converter of a differential input signal to an unipolar signal with a supply voltage peak-to-peak, a prescaler with variable dividing ratio 4/5 and two binary decade counters.
The block is fabricated on TSMC BiCMOS 0.18 um technology.

## 4 STRUCTURE

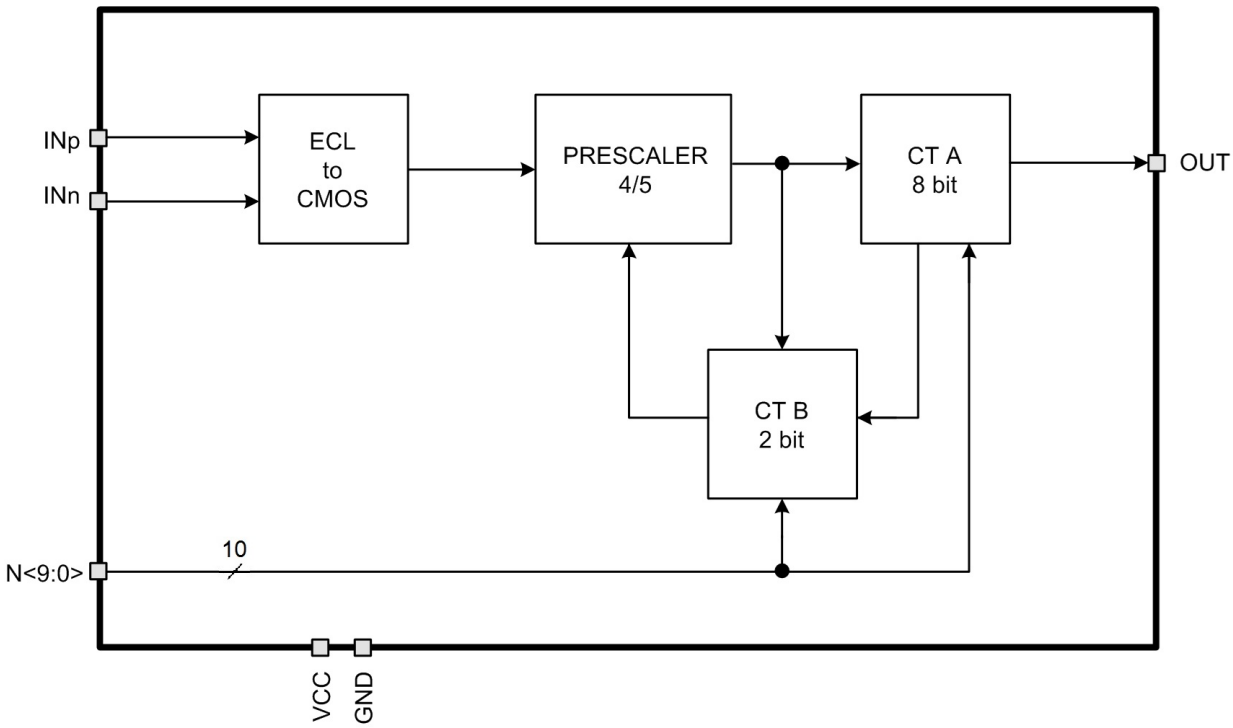


Figure 1: Programmable CMOS PLL high-frequency divider structure

# 5 PIN DESCRIPTION

| Name | Direction | Description |
|---|---|---|
| INp | I | Analog differential input |
| INn | I | |
| N<9:0> | I | Digital code of dividing ratio |
| OUT | O | Divider output |
| VCC | IO | Supply voltage 2.0 V |
| GND | IO | Ground |

# 6 LAYOUT DESCRIPTION

Programmable CMOS PLL high-frequency divider dimensions are given in the table 1.

Table 1: Block dimensions

| Dimension | Value | Unit |
|---|---|---|
| Height | 31 | um |
| Width | 120 | um |

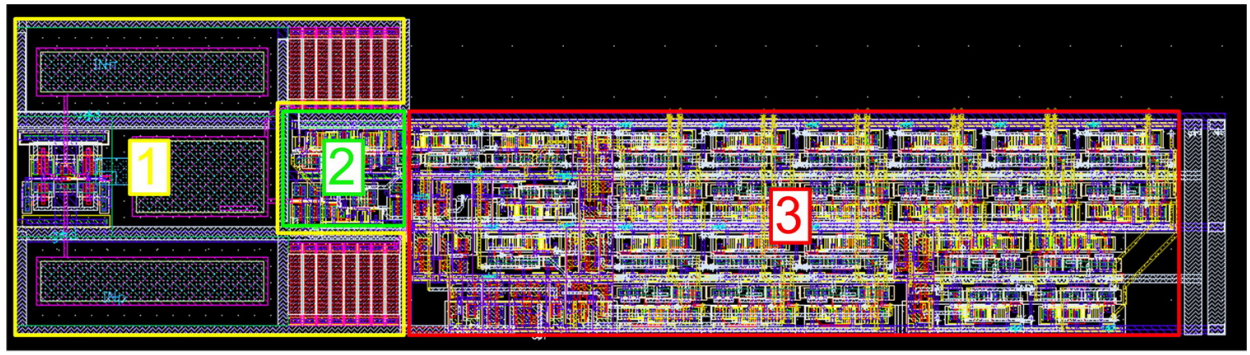


Figure 2: Programmable CMOS PLL high-frequency divider layout

1. ECL/CMOS converter
2. Prescaler with variable dividing ratio 4/5
3. Programmable divider on the basis of two binary decade counters

# 7 OPERATING CHARACTERISTICS

## 7.1 TECHNICAL CHARACTERISTICS

Technology TSMC BiCMOS 0.18 um
Status silicon proven
Area 0.004 $mm^2$

## 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{cc}$ = 1.8 ÷ 2.2 V and $T_j$ = -40 ÷ +85 °C. Typical values are at $V_{cc}$ = 2.0 V, $T_j$ = +27 °C, unless otherwise specified.

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ. | max | |
| Supply voltage | $V_{cc}$ | - | 1.8 | 2 | 2.2 | V |
| Operating temperature range | $T_j$ | - | -40 | +27 | +85 | °C |
| Dividing ratio | R | - | 16 | - | 1023 | - |
| Minimum input frequency | $F_{IN\ MIN}$ | - | - | - | 500 | MHz |
| Maximum input frequency | $F_{IN\ MAX}$ | $V_{cc}$ = 1.8 V | 2100 | - | - | MHz |
| | | $V_{cc}$ = 2.0 V | 2500 | - | - | MHz |
| | | $V_{cc}$ = 2.2 V | 2900 | - | - | MHz |
| Peak-to-peak output voltage | $A_{out\_p\text{-}p}$ | - | 1.8 | 2 | 2.2 | V |
| Peak-to-peak input voltage | $A_{in\ p\text{-}p}$ | - | 0.5 | 0.6 | - | V |
| Supply current | $I_{cc}$ | $F_{IN}$ = 900 MHz | 0.34 | 0.43 | 0.66 | mA |
| | | $F_{IN}$ = 1300 MHz | 0.4 | 0.5 | 0.75 | |
| | | $F_{IN}$ = 1800 MHz | 0.47 | 0.6 | 0.87 | |
| Input logic-level high | $V_{IH}$ | For digital input N<9:0> | $0.9V_{cc}$ | - | $1.1V_{cc}$ | V |
| Input logic-level low | $V_{IL}$ | | -0.2 | - | 0.2 | V |

# 8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation