Programmable CMOS PLL high-frequency divider

SPECIFICATION

1 FEATURES

- TSMC BiCMOS 0.18 um
- Wide range of dividing ratio (56…2047)
- Low current consumption
- Compact structure
- Wide range of operating frequency - up to 5 GHz
- Portable to other technologies (upon request)

2 APPLICATION

- PLL frequency synthesizer

3 OVERVIEW

The CMOS PLL high-frequency divider consists of the converter of a differential input signal to an unipolar signal with a supply voltage peak-to-peak, a prescaler with variable dividing ratio 8/9 and two binary decade counters.
The block is fabricated on TSMC BiCMOS 0.18 um technology.

4 STRUCTURE

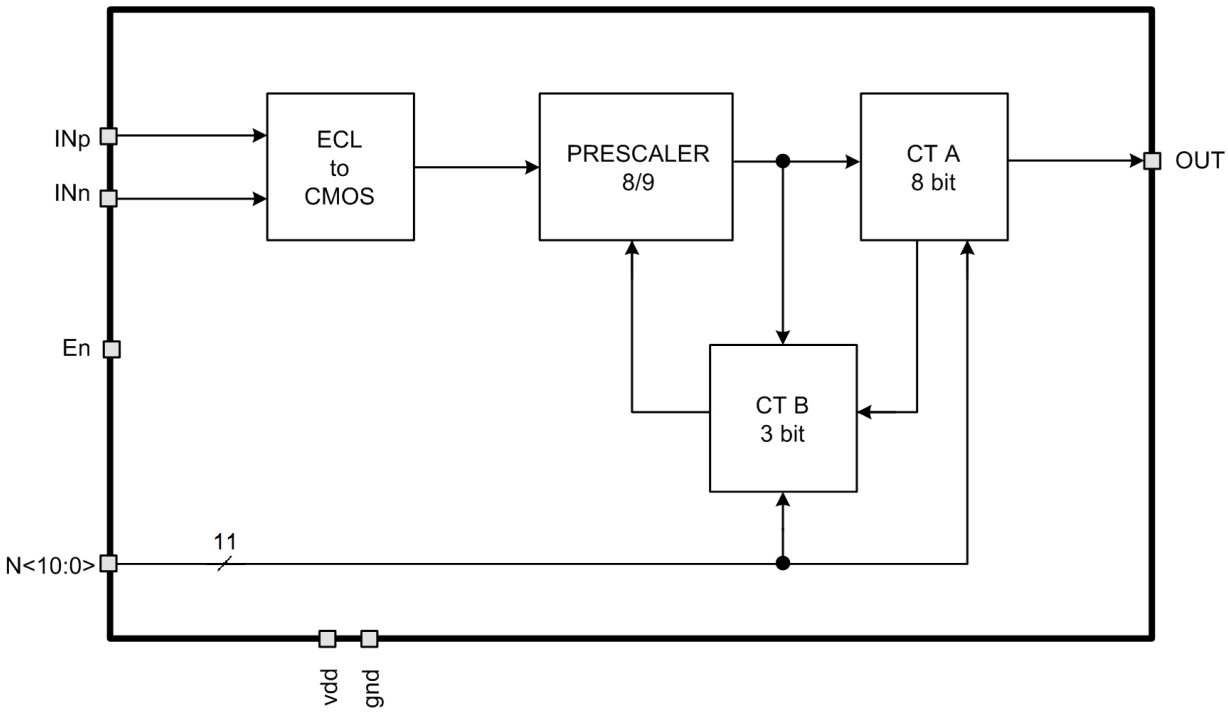

Figure 1: Programmable CMOS PLL high-frequency divider structure

5 PIN DESCRIPTION

Name	Direction	Description
En	I	Enable/disable of divider
INp	I	Analog differential input
INn	I	
N<10:0>	I	Digital code of dividing ratio
OUT	O	Divider output
vdd	IO	Supply voltage 2.0 V
gnd	IO	Ground

6 LAYOUT DESCRIPTION

Programmable CMOS PLL high-frequency divider dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	33	um
Width	120	um

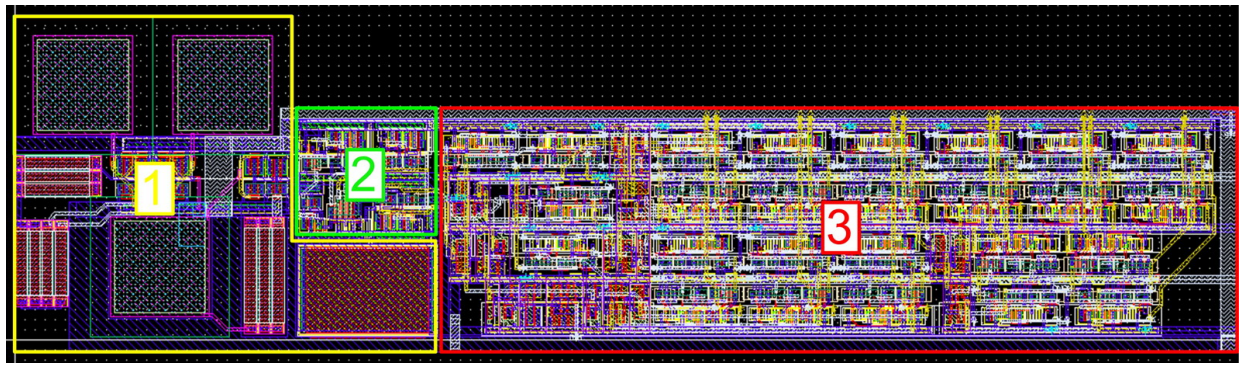

Figure 2: Programmable CMOS PLL high-frequency divider layout

1. ECL/CMOS converter
2. Prescaler with variable dividing ratio 8/9
3. Programmable divider on the basis of two binary decade counters

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC BiCMOS 0.18 um
Status silicon proven
Area 0.004 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.8 ÷ 2.2 V and T_j = -40 ÷ +85 °C. Typical values are at V_{cc} = 2.0 V, T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.8	2.0	2.2	V
Operating temperature range	T_j	-	-40	+27	+85	°C
Dividing ratio	N	-	56	-	2047	-
Minimum input frequency	$F_{IN\ MIN}$	-	-	-	500	MHz
Maximum input frequency	$F_{IN\ MAX}$	V_{cc} = 1.8 V	4400	-	-	MHz
		V_{cc} = 2.0 V	5200	-	-	MHz
		V_{cc} = 2.2 V	6000	-	-	MHz
Peak-to-peak output voltage	$A_{out\_p\text{-}p}$	-	1.8	2	2.2	V
Peak-to-peak input voltage	$A_{in\ p\text{-}p}$	-	0.5	0.6	-	V
Supply current	I_{cc}	F_{IN} = 2600 MHz	1.33	1.91	2.78	uA
		F_{IN} = 3600 MHz	1.48	2.1	3.03	
		F_{IN} = 4400 MHz	1.59	2.26	3.21	
Input logic-level high	V_{IH}	For digital input N<10:0>	$0.9V_{cc}$	-	$1.1V_{cc}$	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation