Programmable CMOS PLL high-frequency divider

SPECIFICATION

1 FEATURES

- TSMC BiCMOS 0.18 um
- Wide range of dividing ratio (21…4097)
- Low current consumption 2.1 mA
- Compact structure
- Portable to other technologies (upon request)

2 APPLICATION

- PLL frequency synthesizer

3 OVERVIEW

The divider consists of the input signal preamplifier (buffer), the converter of a differential input signal to an unipolar signal with a supply voltage peak-to-peak, the prescaler with variable dividing ratio 4/5 and the programmable divider on the basis on two binary decade counters.
The block is fabricated on TSMC BiCMOS 0.18 um.

4 STRUCTURE

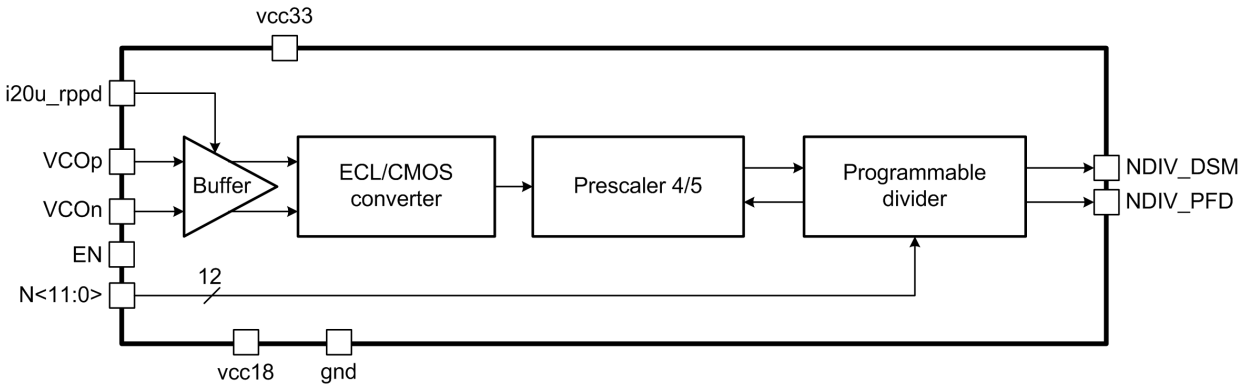

Figure 1: Programmable high-frequency divider structure

5 PIN DESCRIPTION

Name	Direction	Description
i20u_rppd	I	Input signal buffer reference current 20 uA
VCOp	I	Differential analog input
VCOn	I	
EN	I	Enable/disable of divider
N<11:0>	I	Digital code of dividing ratio
NDIV_DSM	O	Divider output to DSM (delta-sigma modulator)
NDIV_PFD	O	Divider output to PFD
vcc33	IO	Supply voltage 3.3 V
vcc18	IO	Supply voltage 1.8 V
gnd	IO	Ground

6 LAYOUT DESCRIPTION

Programmable CMOS PLL high-frequency divider dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	95	um
Width	165	um

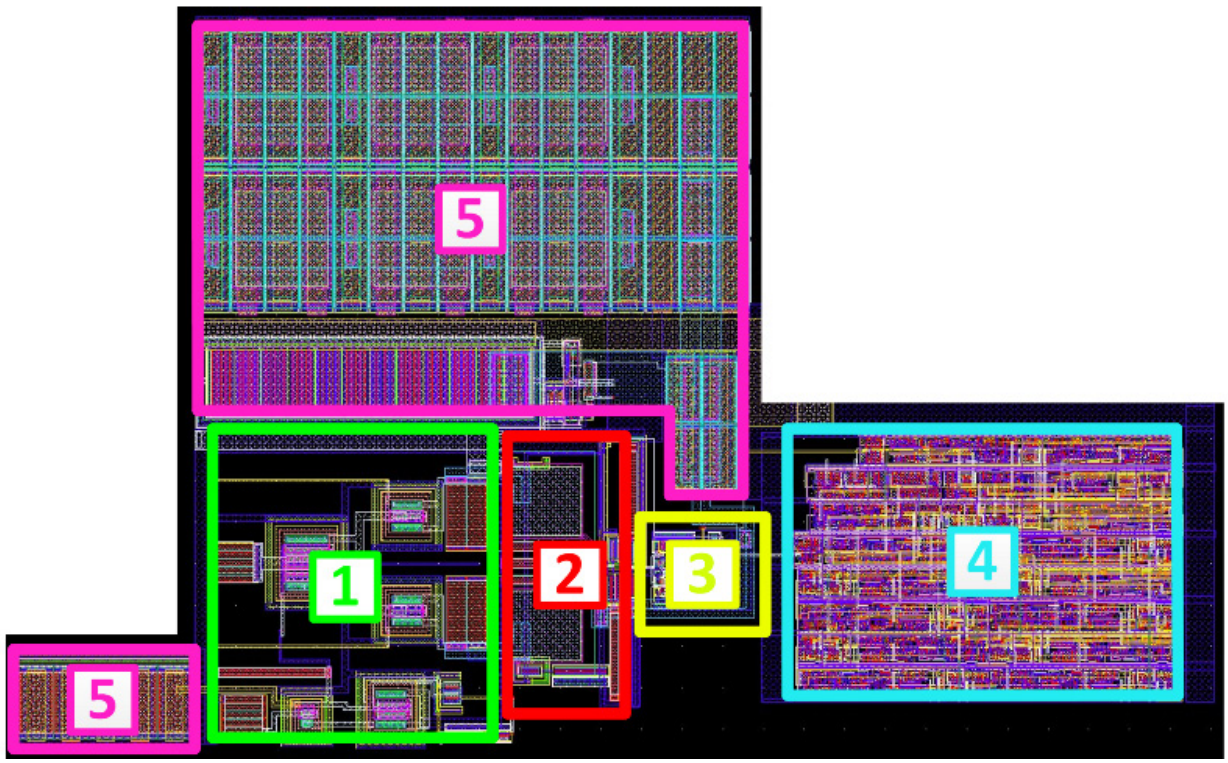

Figure 2: Programmable CMOS PLL high-frequency divider layout

1. Buffer
2. ECL/CMOS converter
3. Prescaler with variable dividing ratio 4/5
4. Programmable divider based on two binary decade counters
5. Filtering capacitors

7 OPERATION CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ TSMC BiCMOS 0.18 um
Status _____ silicon proven
Area _____ 0.015 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc18} = 1.75 ÷ 1.85 V, V_{cc33} = 3.0 ÷ 3.6 V and T_j = -45 ÷ +85 °C, typical values are at V_{cc18} = 1.8 V, V_{cc33} = 3.3 V and T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Input buffer supply voltage	V_{cc33}	-	3.0	3.3	3.6	V
Supply voltage	V_{cc18}	-	1.75	1.8	1.85	V
Operating temperature range	T_j	-	-45	+27	+85	°C
Dividing ratio	N	-	21	-	4097	-
Input frequency range	F	-	2170	-	2500	MHz
Peak-to-peak output voltage	$A_{out\ p\text{-}p}$	-	1.75	1.8	1.85	V
Peak-to-peak input voltage	$A_{in\ p\text{-}p}$	-	0.45	0.6	-	V
Supply current	I_{cc33}	F_{IN} = 2500 MHz	-	2.6	3.5	mA
	I_{cc18}		-	2.1	2.55	
	I_{st}	Stand-by mode	-	20	780	nA
Input logic-level high	V_{IH}	For digital input N<9:0>	$0.9V_{cc}$	-	$1.1V_{cc}$	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V

8 DELIVERABLES

IP block package includes:

- Schematic or NetList
- Abstract model (.lef and .lib files)
- Layout view (optional)
- Behavioral model (Verilog)
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation