Programmable 9-bit CMOS frequency divider

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Range of division ratio from 2 to 511
- Compact structure
- Maximum input frequency 500 MHz
- Portable to other technologies (upon request)

2 APPICATION

- PLL frequency synthesizer

3 OVERVIEW

The programmable CMOS frequency divider is a set of 8 serially connected dividers with the varied division ratio 2/3. This structure is especially effective for wide range of division ratio since the number of triggers to accomplish the specified ratio is minimized. The division ratio is defined by the digital code A<8:0>.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

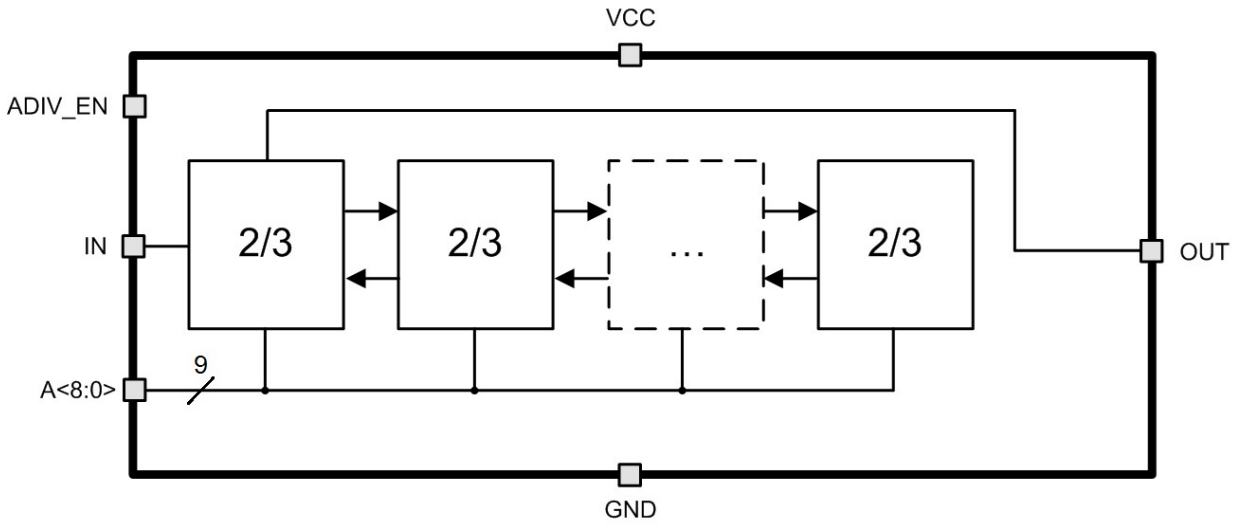

Figure 1: Programmable 9-bit CMOS frequency divider structure

5 PIN DESCRIPTION

Name	Direction	Description
IN	I	Divider input
A<8:0>	I	Digital code of division ratio
ADIV_EN	I	Digital input of divider enabling/disabling
OUT	O	Divider output
VCC	IO	Supply voltage 2 V
GND	IO	Ground

6 LAYOUT DESCRIPTION

Programmable 9-bit CMOS frequency divider dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	30	um
Width	192	um

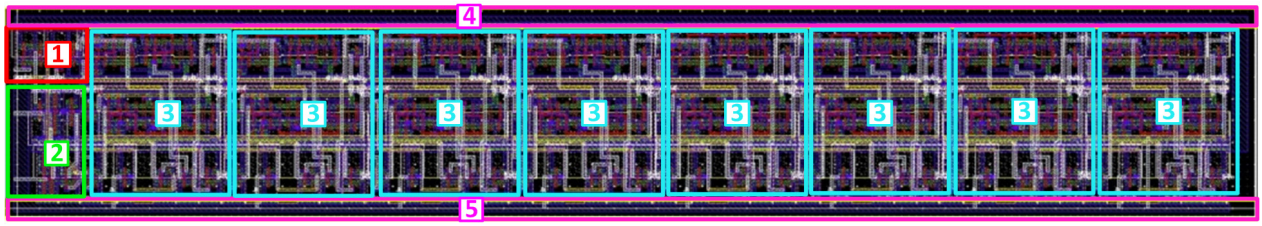

Figure 2: Programmable 9-bit CMOS frequency divider layout

1. Control logic
2. Output buffer
3. Frequency divider 2/3
4. Ground
5. Supply voltage bus

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
Status _____ silicon proven
Area _____ 0.005 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.8 ÷ 2.7 V and T_j = -60 ÷ +125 °C. Typical values are at V_{cc} = 2.0 V and T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.8	2.0	2.7	V
Operating temperature range	T_j	-	-60	27	+125	°C
Division ratio	R	-	2	-	511	-
Input frequency	F_{IN}	-	-	88	500	MHz
Peak-to-peak input voltage	$A_{in\ p\text{-}p}$	-	1.8	2	2.7	V
Peak-to-peak output voltage	$A_{out\_p\text{-}p}$	-	1.8	2	2.7	V
Supply current	I_{cc}	F_{IN} = 88 MHz, F_{out} = 1 MHz	-	45	-	uA
Stand-by current	I_{st}	-	-	1	-	nA
Input logic-level high	V_{IH}	For digital input A <8:0>	$0.9V_{cc}$	-	$1.1V_{cc}$	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V

8 DELIVERABLES

IP block package includes:

- Schematic or NetList
- Abstract model (.lef and .lib files)
- Layout view (optional)
- Behavioral model (Verilog)
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation