Programmable CMOS HF divider

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Wide range of division ratio from 16 to 4095
- Low current consumption
- Compact structure
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- PLL frequency synthesizer

3 OVERVIEW

The programmable CMOS frequency divider consists of two independent circuits. The first one a set of 8 serially connected dividers with the varied division ratio 2/3. This structure is especially effective for wide range of division ratio since the number of triggers to accomplish the specified ratio is minimized. The second divider is based on the prescaler with the varied division ratio 4/5 and the two programmable binary-decimal counters.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

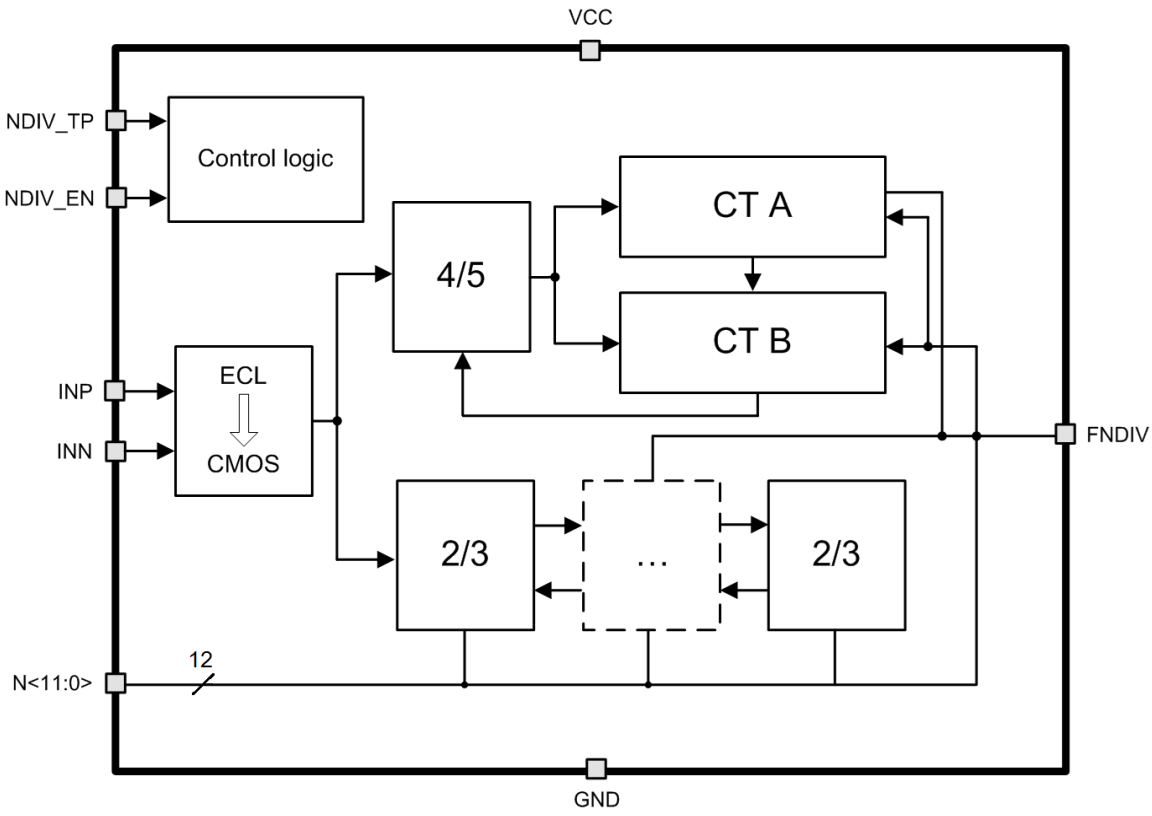

Figure 1: Programmable CMOS HF divider structure

5 PIN DESCRIPTION

Name	Direction	Description
INP	I	Divider differential input
INN	I	
N<11:0>	I	Digital code of division ratio
NDIV_TP	I	Divider type (2/3 or 4/5)
NDIV_EN	I	Enable/disable of divider
FNDIV	O	Divider output
VCC	IO	Supply voltage 2.6 V
GND	IO	Ground

6 LAYOUT DESCRIPTION

Programmable CMOS HF divider dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	90	um
Width	160	um

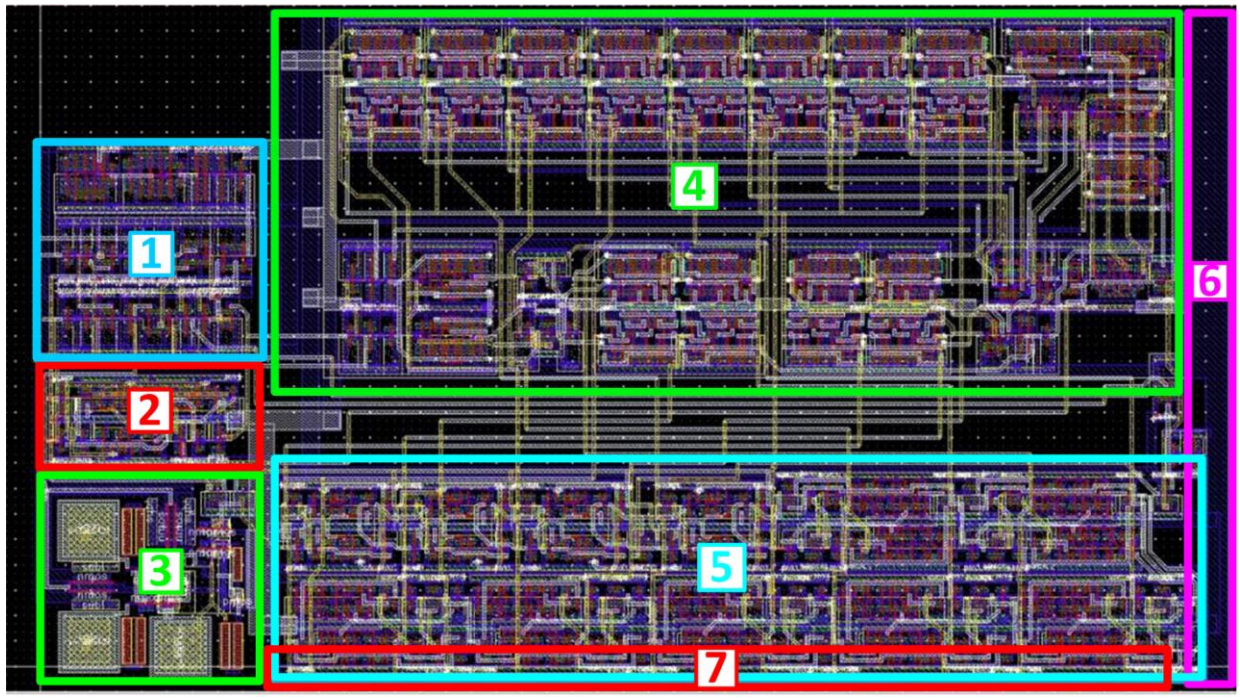

Figure 2: Frequency divider layout

1. Control logic
2. Prescaler 4/5
3. ECL to CMOS converter
4. Programmable divider with binary-decimal counters
5. Frequency divider 2/3
6. Supply voltage bus
7. Ground bus

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
Status _____ silicon proven
Area _____ 0.0144 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.5 ÷ 2.7 V and T_j = -60 ÷ +125 °C. Typical values are at V_{cc} = 2.6 V, T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	2.5	2.6	2.7	V
Operating temperature range	T_j	-	-60	27	+125	°C
Division ratio	R	-	16	-	4095	-
Input frequency	F_{IN}	-	1000	1672	1900	MHz
Peak-to-peak voltage at the differential inputs	A_{div_in}	-	0.5	0.6	-	V
Peak-to-peak output voltage	$A_{out\_p\text{-}p}$	-	2.5	2.6	2.7	V
Supply current	I_{cc}	F_{IN} = 1672 MHz, Divider type "2/3"	-	0.85	-	mA
		F_{IN} = 1672 MHz, Divider type "4/5"		1.22		
Stand-by current	I_{st}	-	-	-	127	nA
Input logic-level high	V_{IH}	For digital inputs	$0.9V_{cc}$	-	$1.1V_{cc}$	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.1:

- Subsection 7.2 update