Programmable CMOS frequency divider

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Wide range of division ratio from 32 to 16383
- Low current consumption
- Compact structure
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra, X-FAB

2 APPLICATION

- PLL frequency synthesizer

3 OVERVIEW

The programmable CMOS frequency divider is a set of serially connected dividers with the varied division ratio 2/3. This structure is especially effective for wide range of division ratio since the number of triggers to accomplish the specified ratio is minimized. The division ratio is defined by the digital code N<13:0>.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

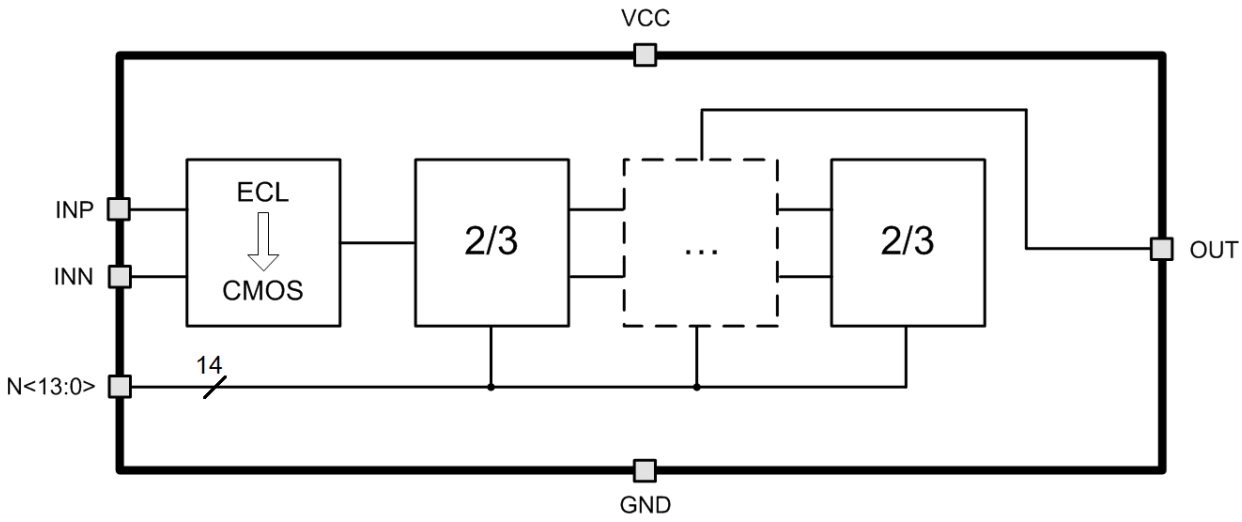

Figure 1: Programmable CMOS frequency divider structure

5 PIN DESCRIPTION

Name	Direction	Description
INP	I	Analog differential input
INN	I	
N<13:0>	I	Digital code of division ratio
OUT	O	Frequency divider output
VCC	IO	Supply voltage 2 V
GND	IO	Ground

6 LAYOUT DESCRIPTION

Programmable CMOS frequency divider dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	175	um
Width	350	um

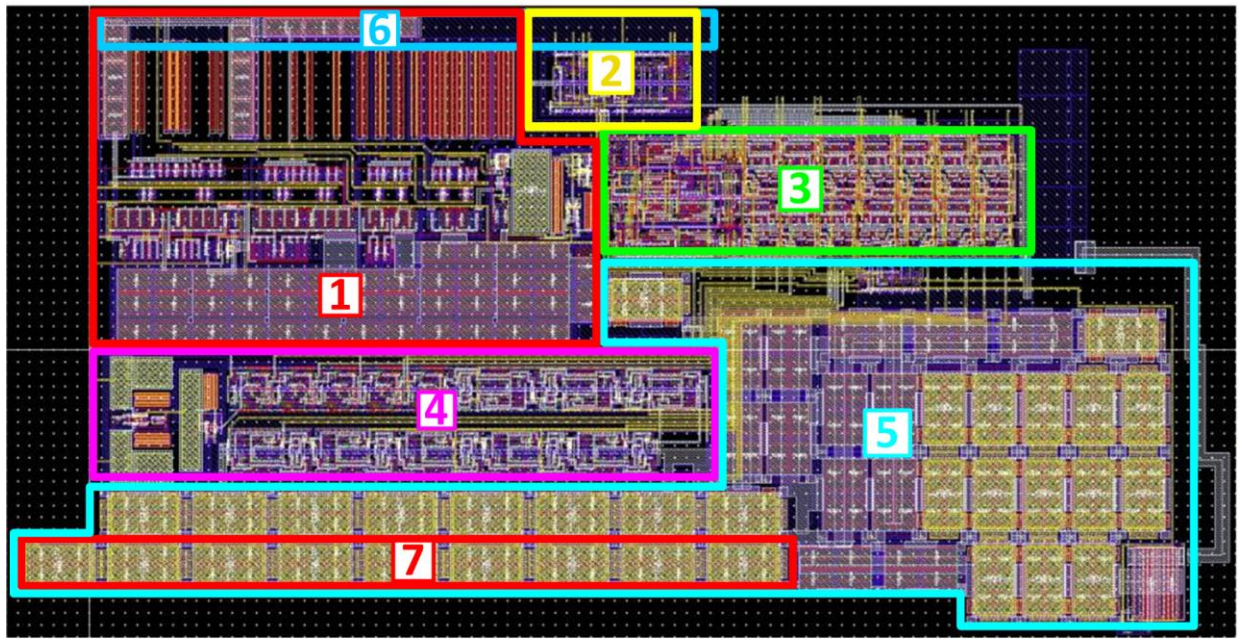

Figure 2: Programmable CMOS frequency divider layout

1. CMOS prescaler 8/9 with commutated current sources
2. Control logic
3. Programmable divider
4. CMOS prescaler 8/9
5. Supply voltage bus filter
6. Supply voltage bus
7. Ground bus

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
Status _____ silicon proven
Area _____ 0.01 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.8 ÷ 2.2 V and T_j = -40 ÷ +85 °C. Typical values are at V_{cc} = 2.0 V, T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.8	2	2.2	V
Operating temperature range	T_j	-	-40	27	+85	°C
Division ratio	R	-	32	-	16383	-
Input frequency	F_{IN}	-	100	435	1050	MHz
Peak-to-peak voltage at the differential inputs	A_{div_in}	-	0.5	0.6	-	V
Peak-to-peak output voltage	$A_{out\_p\text{-}p}$	-	1.8	2	2.2	V
Supply current	I_{cc}	F_{IN} = 140 MHz	-	70	115	uA
		F_{IN} = 435 MHz	-	140	195	
		F_{IN} = 920 MHz	-	250	330	
Stand-by current	I_{st}	-	-	1.65	75	nA
Input logic-level high	V_{IH}	For digital input N<13:0>	0.9V_{cc}	-	1.1V_{cc}	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation