Programmable frequency divider

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Programmable division ratio from 56 to 16383
- Wide frequency range from 50 to 1050 MHz
- Small area
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- PLL frequency synthesizer

3 OVERVIEW

The cell is 14 bit programmable frequency divider fabricated on iHP SGB 0.25 um technology. It consists of ECL prescaler with variable division ratio 8/9 controlled by 3 bit swallow counter and CMOS 11 bit counter. It is characterized by division ratio from 56 to 16383 and current consumption weakly depends on operating frequency.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

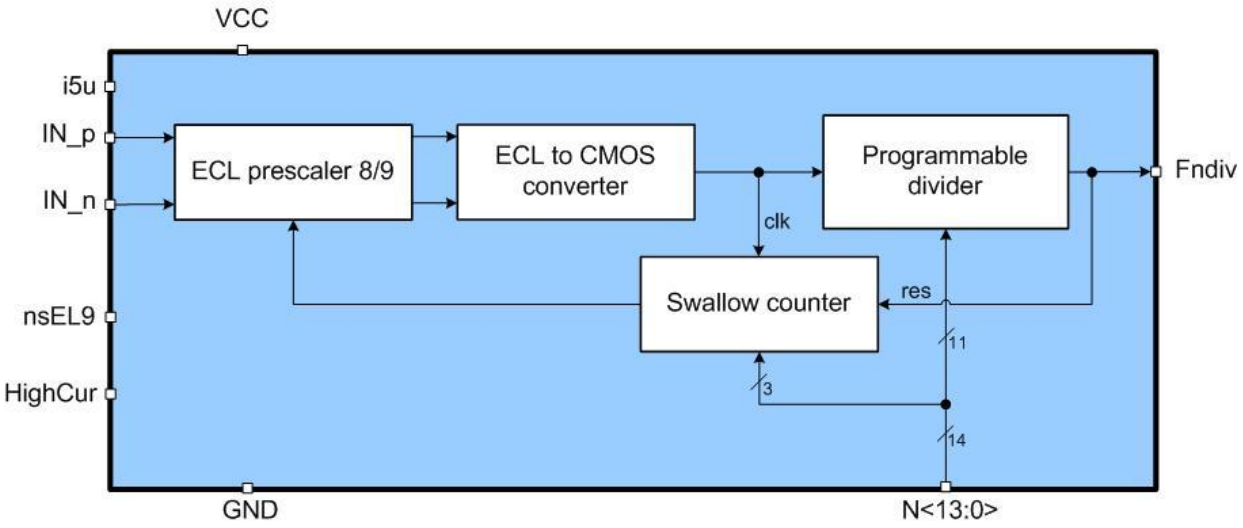

Figure 1: Programmable frequency divider structure

5 PIN DESCRIPTION

Name	Direction	Description
IN_n	I	Analog differential input
IN_p	I	
i5u	I	Reference current 5 uA
nsEL9	I	Swallow counter control
HighCur	I	Current consumption control
N<13:0>	I	Counter division ratio
Fndiv	O	Divider output
VCC	IO	Supply voltage 2.2 V
GND	IO	Ground

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	95.75	um
Width	270	um

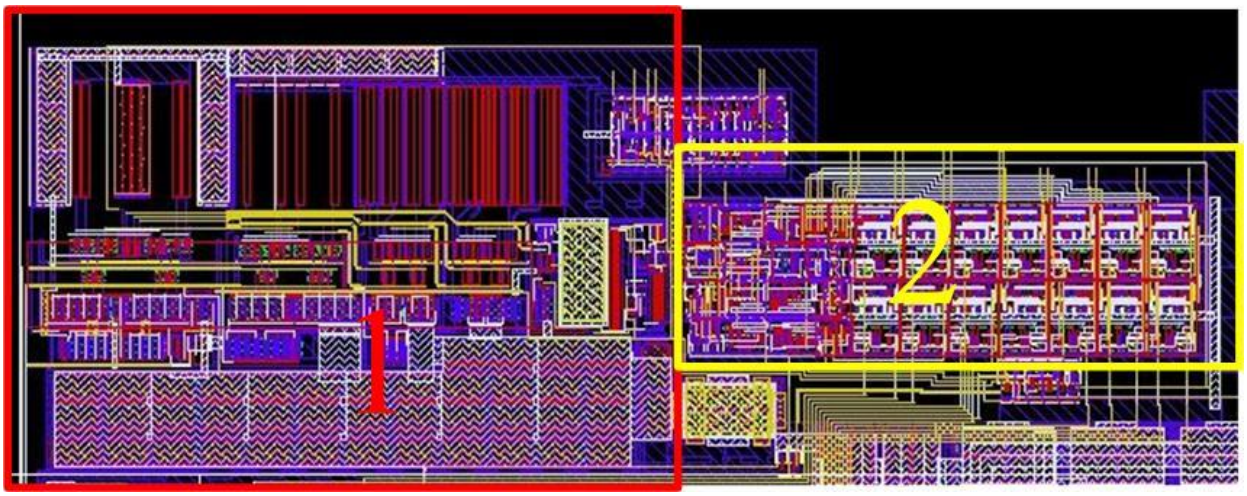

Figure 2: Programmable frequency divider layout

1. ECL prescaler 8/9
2. Programmable divider and swallow counter

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology iHP SiGe BiCMOS 0.25 um
Status silicon proven
Area 0.025 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.9 ÷ 2.3 V and T_j = -45 ÷ +85 °C. Typical values are at V_{cc} = 2.2 V and T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.9	2.2	2.3	V
Operating temperature range	T_j	-	-45	27	85	°C
Division ratio	N	-	56	-	16383	-
Operating frequency range	F	-	50	-	1050	MHz
Peak-to-peak differential input voltage*	$A_{in\ p\text{-}p}$	F = 140 MHz	-	400	-	mV
		F = 435 MHz	-	600	-	mV
		F = 930 MHz	-	840	-	mV
Peak-to-peak output voltage*	$A_{out\ p\text{-}p}$	CMOS	1.9	2.2	2.3	V
Supply current	I_{cc}	F = 140 MHz	285	292	302	uA
		F = 435 MHz	300	306	315	
		F = 930 MHz	364	372	390	
Stand-by current	I_{stb}	-	-	20	54	nA
Input logic-level high	V_{IH}	For digital inputs	$0.7V_{cc}$	-	V_{cc}+0.25	V
Input logic-level low	V_{IL}		-0.25	-	0.3	V

* DC coupled

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation