

# 9-bit programmable ECL high-frequency divider

## SPECIFICATION

### 1 FEATURES

- AMS BiCMOS 0.35  $\mu\text{m}$
- Differential structure
- Dividing ratio is regulated in the range of 8 ... 511 with step 1
- Input differential signal frequency up to 1.7 GHz
- Scalable structure
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SiTerra, X-FAB

### 2 APPLICATION

- PLL frequency synthesizer

### 3 OVERVIEW

The 9-bit programmable ECL high-frequency divider is a set of serially connected dividers with the varied dividing ratio  $2/3$  that is able to scale the structure either into minimum dividing ratio decreasing or maximum dividing ratio increasing. The differential circuit has higher noise immunity.

The block is fabricated on AMS BiCMOS 0.35  $\mu\text{m}$  technology.

### 4 STRUCTURE

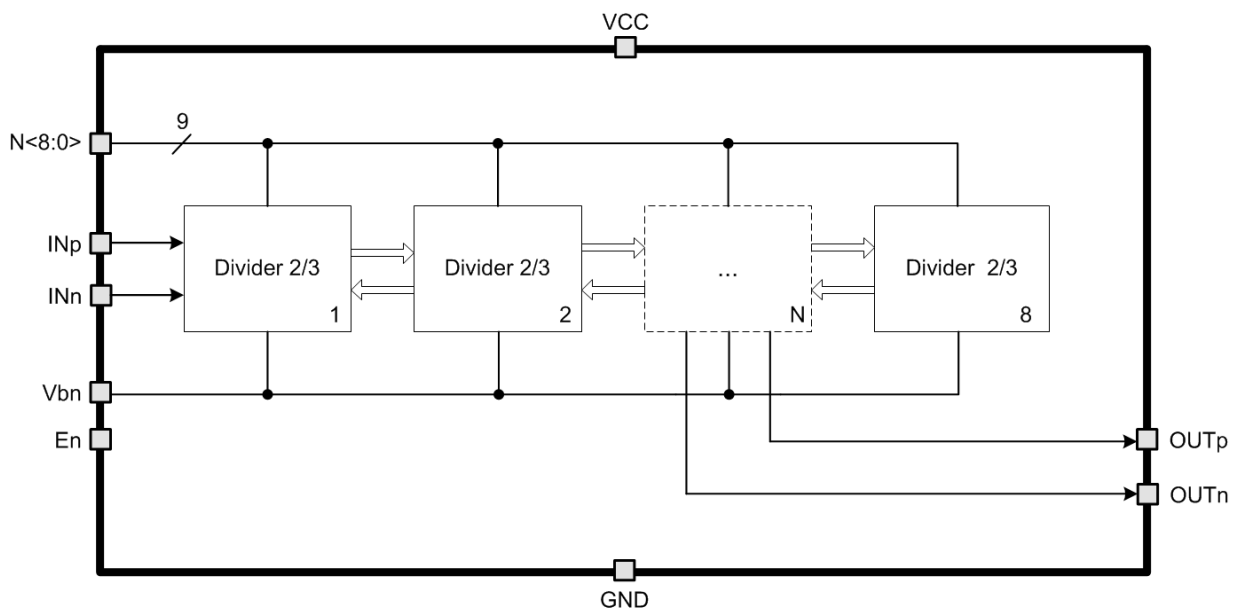


Figure 1: 9-bit programmable ECL high-frequency divider structure

## 5 PIN DESCRIPTION

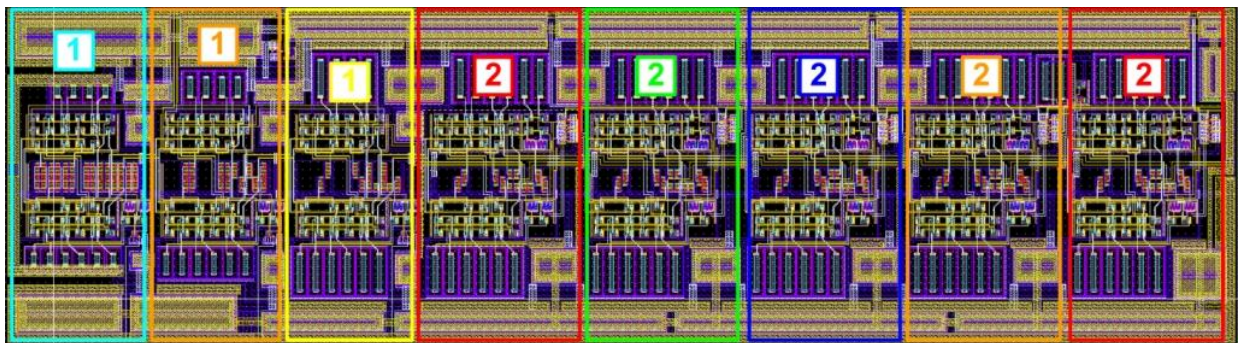
Name	Direction	Description
INp	I	Analog differential input
INn	I	
N<8:0>	I	Digital code of dividing ratio
Vbn	I	Reference voltage of current source
En	I	Enable/disable of divider
OUTp	O	Analog differential output
OUTn	O	
VCC	IO	Supply voltage 2.7 V
GND	IO	Ground

## 6 LAYOUT DESCRIPTION

9 bit programmable ECL high-frequency divider dimensions are given in the table 1.

**Table 1:** Block dimensions

Dimension	Value	Unit
Height	235	um
Width	858	um



**Figure 2:** Block layout

1. Frequency divider 2/3
2. Frequency divider 2/3 with control logic

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ AMS BiCMOS 0.35  $\mu\text{m}$   
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_ 0.202  $\text{mm}^2$

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc} = 2.4 \div 3.6 \text{ V}$ ,  $T_j = -40 \div +85 \text{ }^\circ\text{C}$ . Typical values are at  $V_{cc} = 2.7 \text{ V}$ ,  $T_j = +27 \text{ }^\circ\text{C}$ , unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	$V_{cc}$	-	2.4	2.7	3.6	V
Operating temperature range	$T_j$	-	-40	+27	+85	$^\circ\text{C}$
Dividing ratio	N	-	8	-	511	-
Input frequency	$F_{IN}$	-	-	-	1.7	GHz
Peak-to-peak input voltage	$A_{in\ p-p}$	At differential input	0.4	-	1	V
In-phase component of input signal	$A_{in\ dc}$	$V_{cc}=2.7 \text{ V}$	1.6	1.8	2	V
Peak-to-peak output voltage	$A_{out\ p-p}$	An differential output	0.3	0.4	0.55	V
In-phase component of output signal	$A_{out\ dc}$	$V_{cc}=2.7 \text{ V}$	1.6	1.8	2	V
Supply current	$I_{cc}$	-	-	2	-	mA
Stand-by current	$I_{st}$	-	-	15	110	nA
Input logic-level high	$V_{IH}$	-	$0.9V_{cc}$	-	$V_{cc}$	V
Input logic-level low	$V_{IL}$	-	-0.2	0	0.2	V

## 8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

## REVISION HISTORY

1. From version 1.0:
  - Section “Technical characteristics” (refer to [page 3](#))