5-bit programmable CMOS low-frequency divider

SPECIFICATION

1 FEATURES

- TCMS BiCMOS 0.18 um
- Continued range of dividing ratio (1…31)
- Low current consumption
- Compact structure
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- PLL frequency synthesizer

3 OVERVIEW

The 5-bit programmable CMOS low-frequency divider consists of an asynchronous pulse counter, a control logic and a multiplexer that is able to commutate an input signal to output.
The block is fabricated on TCMS BiCMOS 0.18 um technology.

4 STRUCTURE

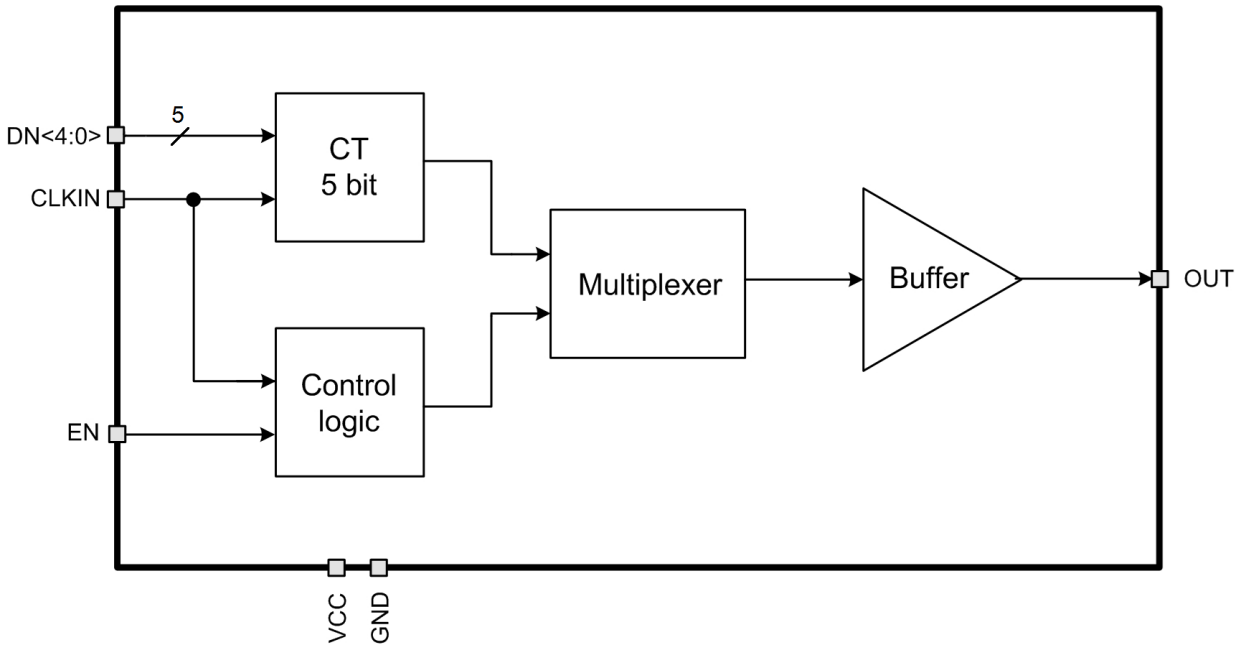

Figure 1: 5-bit programmable CMOS low-frequency divider structure

5 PIN DESCRIPTION

Name	Direction	Description
CLKIN	I	Divider input
DN<4:0>	I	Digital code of dividing ratio
EN	I	Enable/disable of divider
OUT	O	Divider output
VCC	IO	Supply voltage 1.8 V
GND	IO	Ground

6 LAYOUT DESCRIPTION

5 bit programmable CMOS low-frequency divider dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	30	um
Width	60	um

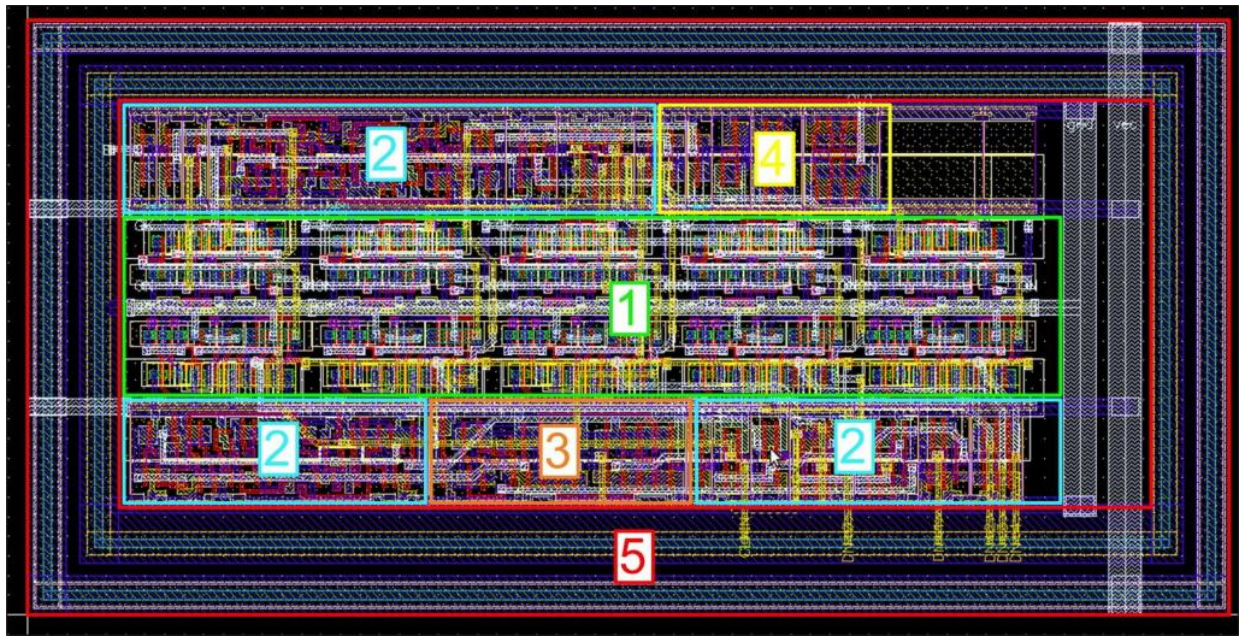

Figure 2: Programmable CMOS PLL high-frequency divider layout

1. 5-bits asynchronous counter
2. Control logic
3. Multiplexer
4. Output buffer
5. Guard ring

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC 0.18 um
Status silicon proven
Area 0.002 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.0 ÷ 2.2 V and T_j = -40 ÷ +85 °C. Typical values are at V_{cc} = 1.8 V, T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.0	1.8	2.2	V
Operating temperature range	T_j	-	-40	+27	+85	°C
Dividing ratio	R	-	1	-	31	-
Maximum input frequency	$F_{IN\ MAX}$	V_{cc} = 1.0 V	200	-	-	MHz
		V_{cc} = 1.4 V	500	-	-	MHz
		V_{cc} = 1.8 V	800	-	-	MHz
Supply current	I_{cc}	F_{IN} = 50 MHz, R = 5	-	20	-	uA
Stand-by current	I_{sb}	-	-	1.2	-	nA
Input logic-level high	V_{IH}	For digital input DN<4:0>	0.9V_{cc}	-	1.1V_{cc}	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation