Programmable 5-bit CMOS low-frequency divider

SPECIFICATION

1 FEATURES

- TSMC SiGe BiCMOS 0.18 um
- Range of division ratio from 1 to 31
- Low current consumption 10 uA
- Portable to other technologies (upon request)

2 APPLICATION

- PLL frequency synthesizer

3 OVERVIE

The programmable CMOS low-frequency divider configuration of asynchronous programmable impulse counter, control logic and output buffer.
The block is fabricated on TSMC SiGe BiCMOS 0.18 um.

4 STRUCTURE

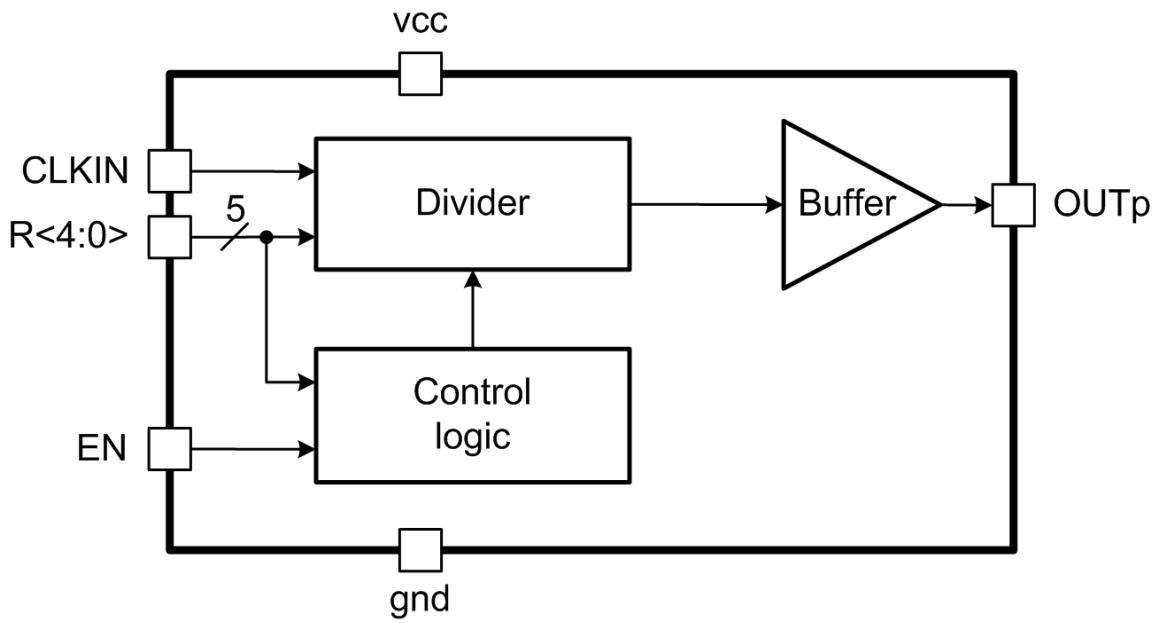

Figure 1: Programmable 5-bit CMOS low-frequency divider structure

5 PIN DESCRIPTION

Name	Direction	Description
CLKIN	I	Digital input
R<4:0>	I	Digital code of division ratio
EN	I	Divider enable/disable
OUTp	O	Divider linear output
vcc	IO	Supply voltage 3.3 V
gnd	IO	Ground

6 LAYOUT DESCRIPTION

Programmable 5-bit CMOS low-frequency divider dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	28	um
Width	70	um

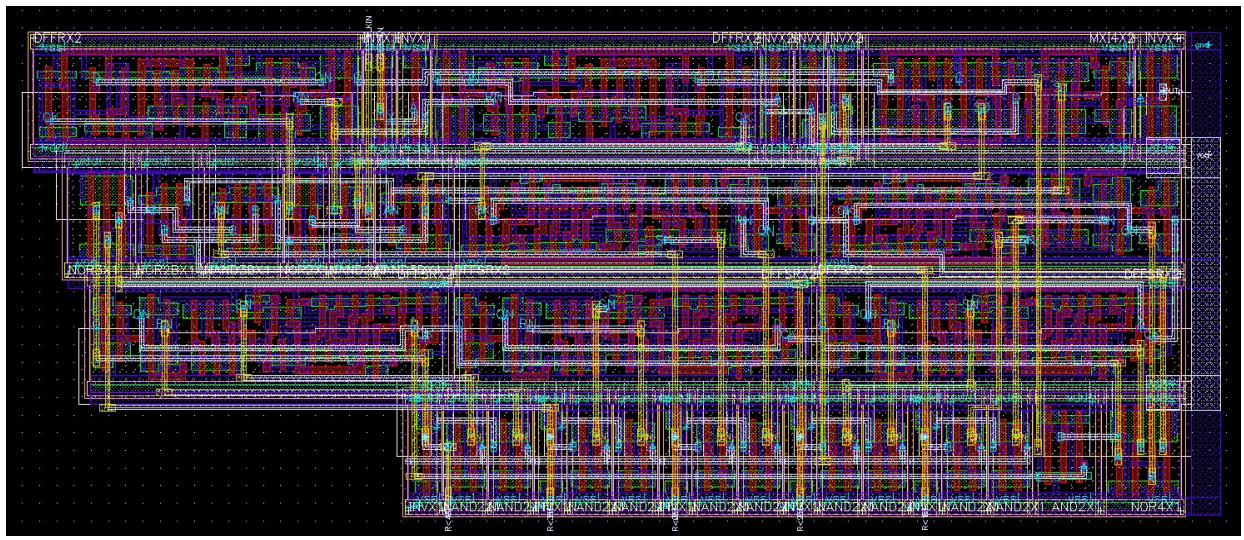

Figure 2: Programmable 5-bit CMOS low-frequency divider layout

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC SiGe BiCMOS 0.18 um
Status silicon proven
Area 0.002 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 3.0 ÷ 3.6 V and T_j = -45 ÷ +85 °C. Typical values are at V_{cc} = 3.3 V and T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	3.0	3.3	3.6	V
Operating temperature range	T_j	-	-45	+27	+85	°C
Division ratio	R	-	1	-	31	-
Input frequency	F_{IN}	-	0	-	60	MHz
Supply current	I_{cc}	F_{IN} = 44 MHz, R = 1;2	-	10	20	uA
		F_{IN} = 44 MHz, R = 3-31	-	30	45	uA
Stand-by current	I_{sb}	-	-	0.05	3.0	nA
Input logic-level high	V_{IH}	For digital inputs R<4:0>	$0.9V_{cc}$	-	$1.1V_{cc}$	V
Input logic-level low	V_{IL}		-0.2	-	0.2	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation