4-bit programmable ECL low-frequency divider

SPECIFICATION

1 FEATURES

- AMS BiCMOS 0.35 um
- Differential structure
- Dividing ratio is regulated in the range of 1…15 with step 1
- Input differential signal frequency up to 150 MHz
- Scalable structure
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra, X-FAB

2 APPLICATION

- PLL frequency synthesizer

3 OVERVIEW

The 4-bit programmable ECL low-frequency divider is a set of serially connected dividers with the varied dividing ratio 2/3 that is able to scale the structure into maximum dividing ratio increasing. If a dividing ratio is set to 1, an input signal is switched to output and the circuit is disabled. The differential circuit has higher noise immunity.
The block is fabricated AMS035 BiCMOS 0.35 um technology.

4 STRUCTURE

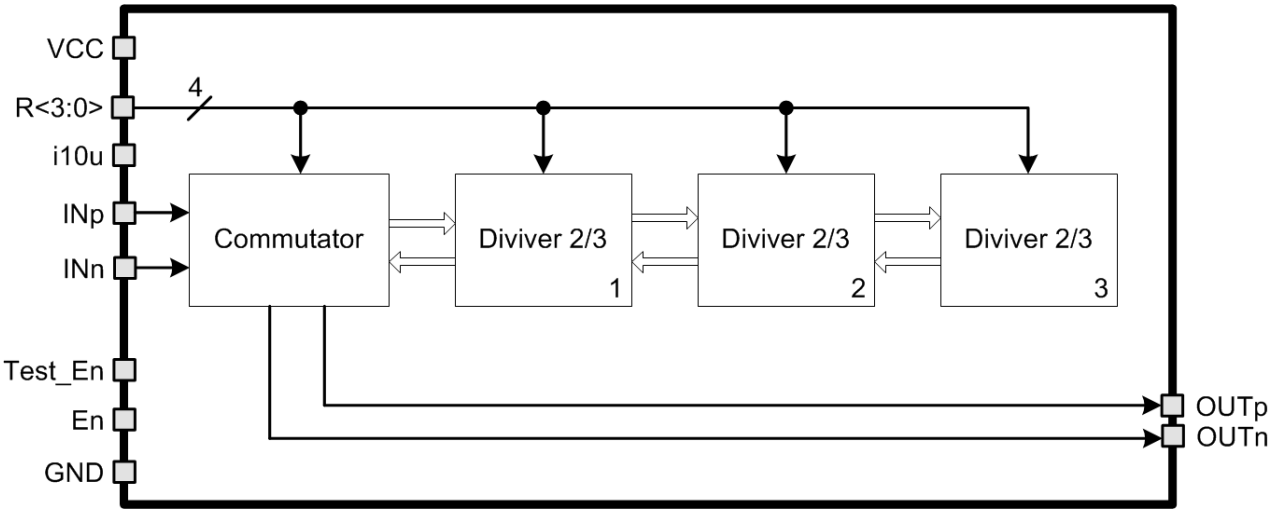

Figure 1: 4-bit programmable ECL low-frequency divider structure

5 PIN DESCRIPTION

Name	Direction	Description
INp	I	Analog differential input
INn	I	
R<3:0>	I	Digital code of dividing ratio
i10u	I	Reference current 10 uA
En	I	Enable/disable of divider
Test_En	I	Enable/disable of divider test mode
OUTp	O	Analog differential output
OUTn	O	
VCC	IO	Supply voltage 2.7 V
GND	IO	Ground

6 LAYOUT DESCRIPTION

4-bit programmable ECL low-frequency divider dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	298	um
Width	426	um

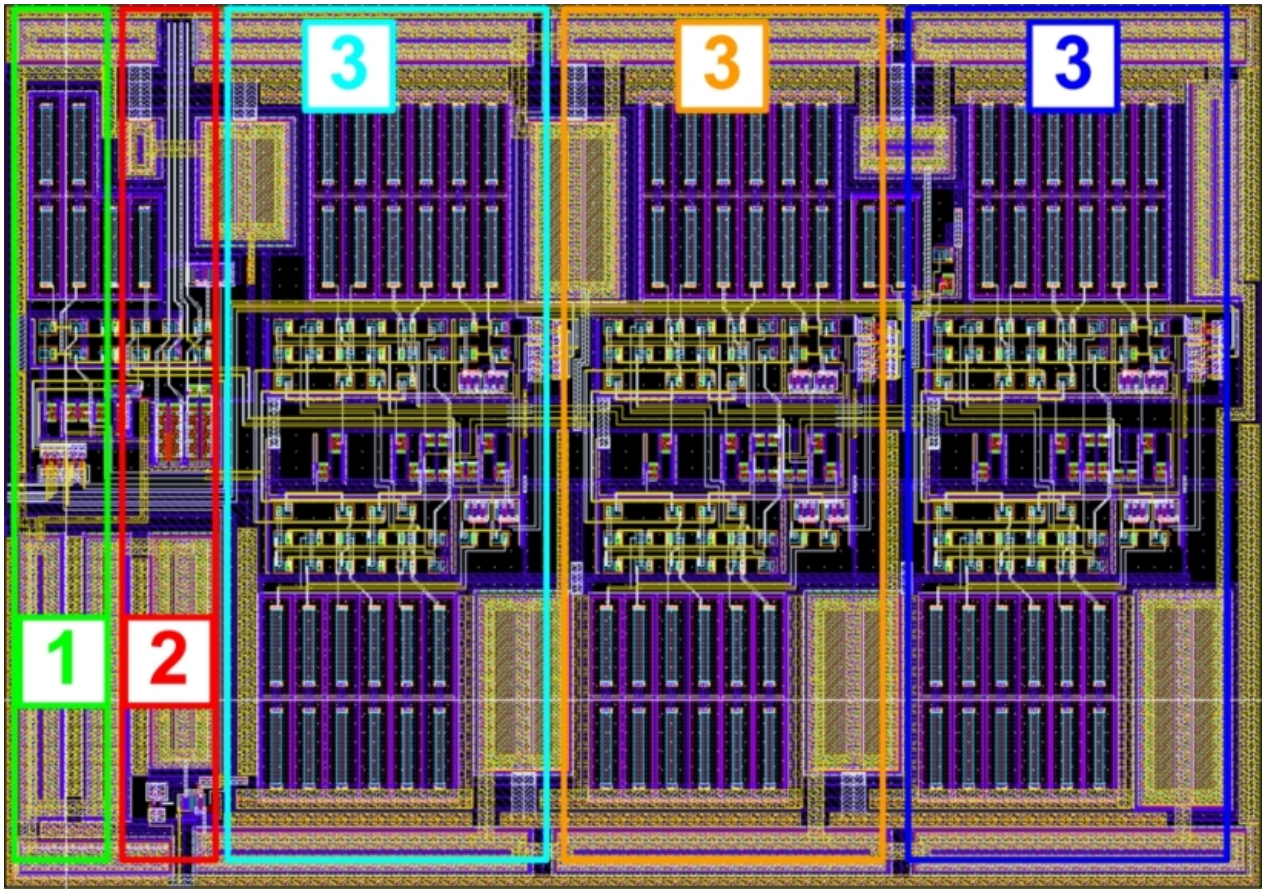

Figure 2: 4-bit programmable ECL low-frequency divider layout

1. Input amplifier
2. Output buffer-commutator
3. Frequency divider 2/3

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology AMS035 BiCMOS 0.35 um
Status silicon proven
Area 0.127 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 2.4 ÷ 3.3 V and T_j = -40 ÷ +85 °C. Typical values are at V_{cc} = +2.7 V and T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Conditions	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	2.4	2.7	3.3	V
Operating temperature range	T_j	-	-40	27	+85	°C
Dividing ratio	R	-	1	-	15	-
Input frequency	F_{IN}	-	5	-	150	MHz
Peak-to-peak input voltage	$A_{in\ p\text{-}p}$	At differential input	0.3	0.4	0.8	V
In-phase component of input signal	$A_{in\ dc}$	V_{cc} = 2.7 V	1.6	2	2.4	V
Peak-to-peak output voltage	$A_{out\_p\text{-}p}$	An differential output	0.3	0.4	0.55	V
In-phase component of output signal	$A_{out\ dc}$	V_{cc} = 2.7 V	1.6	1.8	2	V
Supply current	I_{cc}	R-divider ratio =1	-	0.15	-	mA
		R-divider ratio =2 …15	-	0.47	-	
Stand-by current	I_{st}	-	-	6	60	nA
Input logic-level high	V_{IH}	-	0.9V_{cc}	-	V_{cc}	V
Input logic-level low	V_{IL}	-	-0.2	0	0.2	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation