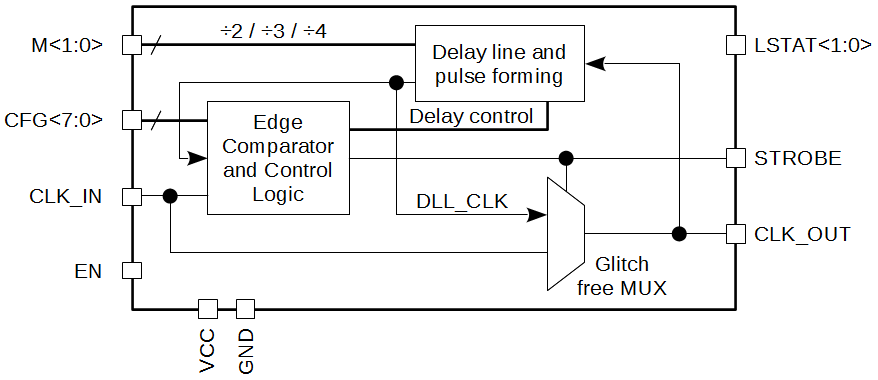
10 – 200 MHz DLL-based frequency multiplier

OVERVIEW

DLL-based frequency multiplier is a simple to configure and operate block, combining, small area and low current consumption. Block wakes up in “pass-through” mode with redirecting input reference frequency to the output. After being configured and enabled the block waits until DLL locks and then switches output clock signal CLK_OUT to higher frequency. Disabling block switches it back to “pass-through” mode. Any mode switching is glitch-protected.



IP technology: GlobalFoundries 55 nm.
IP status: silicon proven.
Layout dimensions: 0.440x0.209mm. Total area: 0.092 mm^2.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition		Value min	Value typ.	Value max	Unit
Supply voltage	V_{CC}	Core voltage		1.1	1.2	1.3	V
Die temperature	T_j	-		-40	27	125	°C
Block current consumption	$I_{STARTUP}$	During 1us after signal EN goes from signal pass-through to DLL clock output		-	-	4	mA
	I_{ACTIVE}	Active mode F_{CLK_OUT}=200MHz		-	230	490	uA
	I_{PASS}	Pass through mode, signal pass-through	F_{REF_IN}=10MHz	-	5	20	
			F_{REF_IN}=50MHz	-	25	40	
			F_{REF_IN}=100MHz	-	40	70	
		Pass through mode, DLL clock output, M = 1	F_{REF_IN}=10MHz	-	140	250	
			F_{REF_IN}=50MHz	-	220	400	
			F_{REF_IN}=100MHz	-	290	490	
Reference frequency range	F_{CLK_IN}	-		0.01	-	100	MHz
CLK_OUT max frequency	F_{OUTMAX}	-		200	-	-	MHz
CLK_OUT min frequency	F_{OUTMIN}	Note1		11.5	18	26	MHz
		Note2		5	8	13	
		Note3		9	16	23	
		Note4		2.5	4	7.5	
CLK_IN duty cycle	CKI_{DC}	-		40	50	60	%
CLK_OUT duty cycle	CKO_{DC}	DLL is locked		40	50	60	%
Delay between rising edge of CLK_IN and following rising edge of CLK_OUT	T_{LATIO}	-		-	0.270	0.5	ns
CLK_IN period jitter[1)]	T_{J_IN}	-		-	200	-	ps
CLK_OUT period jitter[1)] with power supply noise	T_{JPSN}	M=4	F_{CLK_OUT}=4MHz	-	8	-	ns
			F_{CLK_OUT}=12MHz	-	3	-	
			F_{CLK_OUT}=24MHz	-	1.6	-	
			F_{CLK_OUT}=48MHz	-	0.7	-	
			F_{CLK_OUT}=100MHz	-	0.4	-	
			F_{CLK_OUT}=200MHz	-	0.3	-	
Input logic-high level	V_{IH}	For digital inputs		0.8*V_{CC}	-	V_{CC}+0.1	V
Input logic-low level	V_{IL}			-0.1	-	0.2*V_{CC}	V

Note: 1) Absolute value of period deviation from period nominal (expected) value