800 MHz DLL-based frequency multiplier

SPECIFICATION

1 FEATURES

- TSMC CMOS LP 90 nm
- Low jitter
- Precisely aligns the clock distribution output with a reference clock
- Low current consumption
- Compact implementation of the lowpass filter
- Supported foundries: TSMC, UMC, Global Foundries, SMIC

2 APPLICATION

- Frequency synthesizer

3 OVERVIEW

Multiplying delay-locked loop (MDLL) clock multiplier accept an input clock and generates a phase-locked output clock at a multiple of the input clock frequency. As with a DLL, each rising edge of the input clock zeros the phase error of the loop. Hence this circuit combines the low phase noise of a DLL with the clock multiplication ability of a PLL. A divide-by-M counter provides a programmable multiplication ratio for the MDLL.
The block fabricated on TSMC CMOS Logic Process 90 nm.

4 STRUCTURE

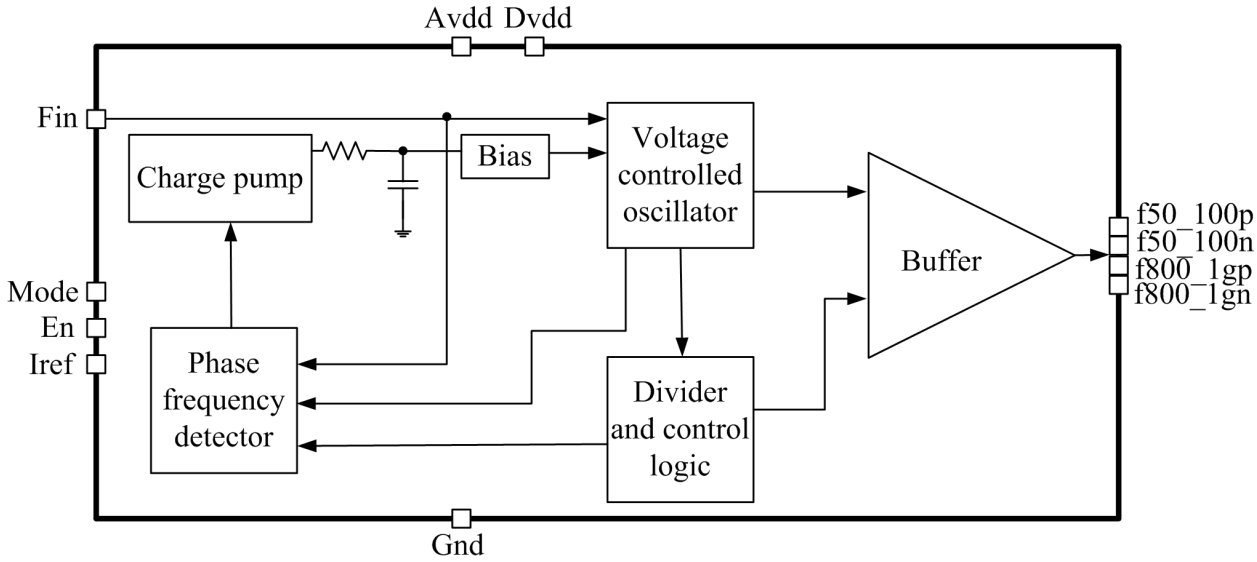

Figure 1: Multiplying delay-locked loop structure

5 PIN DESCRIPTION

Name	Direction	Description
Iref	I	Input current
Fin	I	Input reference clock
Mode	I	Mode («0» – 800 MHz, «1» – 1 GHz)
En	I	Enable
f50_100p	O	Output clock 50 MHz (100 MHz)
f50_100n	O	Inversion output clock 50 MHZ (100 MHz)
f800_1gp	O	Output clock 800 MHz (1 GHz)
f800_1gn	O	Inversion output clock 800 MHz (1 GHz)
Avdd	I/O	Digital blocks supply voltage 1 V
Dvdd	I/O	Analog blocks supply voltage 1 V
Gnd	I/O	Ground

6 LAYOUT DESCRIPTION

Programmable CMOS multiplying delay-locked loop dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	70	um
Width	50	um

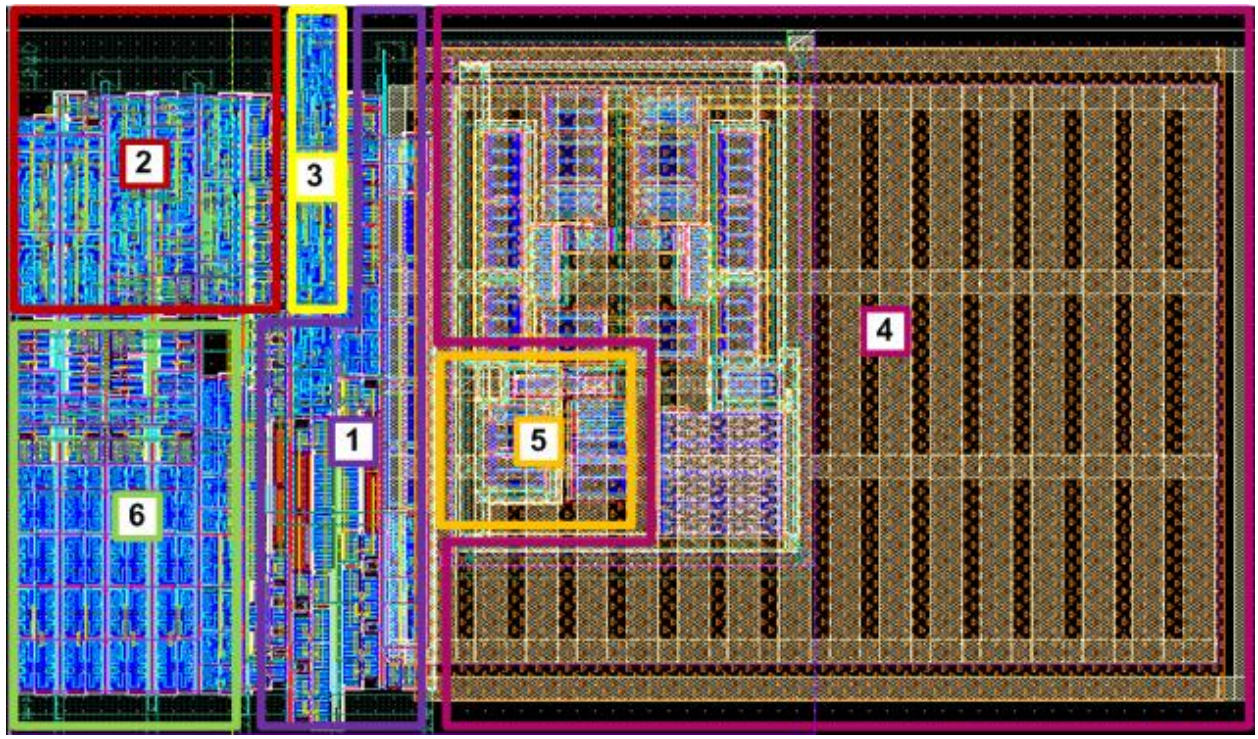

Figure 2: Multiplying delay-locked loop layout

1. Voltage controlled oscillator
2. Divider and control logic
3. Phase frequency detector
4. Charge pump and low pass filter
5. Bias
6. Buffer

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC CMOS LP 90 nm
Status silicon proven
Area 0.0035 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{dd} = 0.95 \div 1.05$ V and $T_j = -40 \div +125$ °C. Typical values are at $V_{dd} = 1$ V, $T_j = +27$ °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{dd}	-	0.95	1	1.05	V
Power	P_{dd}	$F_{800\_1g} = 1$ GHz	0.95	1	1.05	mW
Operating temperature range	T_j	-	-40	27	125	°C
Multiplying ratio	N	-	-	16/20	-	-
Output frequency	F_{800_1g}	-	-	800 (1000)	-	MHz
Output duty cycle	S	-	-	51	-	%
Jitter (root mean square)	J	$F_{800\_1g} = 1$ GHz	5.5	6	6.5	ps
Lock time	T_{lock}	-	2	5	10	us
Input logic-level high	V_{IH}	For digital inputs	0.7	-	-	V
Input logic-level low	V_{IL}		-	-	0.3	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation