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# Intermediate frequency amplifier

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## SPECIFICATION

### 1 FEATURES

- SMIC CMOS 0.18 um
- Wide gain range (0...62 dB)
- Low input noise figure
- Low group delay time ripple vs. frequency and gain
- Digital and analog output modes
- Built-in AGC detector without external capacitor
- No external components required
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, SilTerra

### 2 APPLICATION

- Receivers
- Transceivers
- Navigation systems

### 3 OVERVIEW

The device is a dual intermediate-frequency amplifier (IFA) which consists of 4 stages amplifier with tunable gain, an input linear buffer for analog output and an analog-digital converter for digital output and a detector of output level.

The amplifier has differential inputs and outputs, and consists of 4 stages. Gain is sequentially reduced from the last stage to the first stage. This method allows to keep a low noise figure in wide gain range.

The amplifier can operate in the following modes:

- Linear output with automatic gain control (AGC)
- Digital output with AGC for analog signal
- Digital output with AGC for digital signal

In the analog output mode the circuit retains a low output offset voltage and controls the gain so that the magnitude of the differential output signal is 200 mV peak-to-peak. DC offset compensation system operates both at an amplifier output signal and at a buffer output signal.

Digital output with AGC for analog signal mode operates similarly to the previous mode, through the output signal is converted by ADC. 2-bit ADC consists of three comparators (a one registers "0", the rest operate at certain positive and negative threshold crossing). Encoder is used to transmit signals from the three comparators, through two outputs. The encoder has outputs SIGN and MAGN

In the digital output with AGC for digital signal mode compensation system uses zero transient comparator signal (SIGN). AGC operates in an automatic control mode of digital detector threshold for digital signal (MAGN). Threshold and gain are set by the DAC code.

The block is fabricated on SMIC CMOS 0.18 um technology.

## 4 STRUCTURE

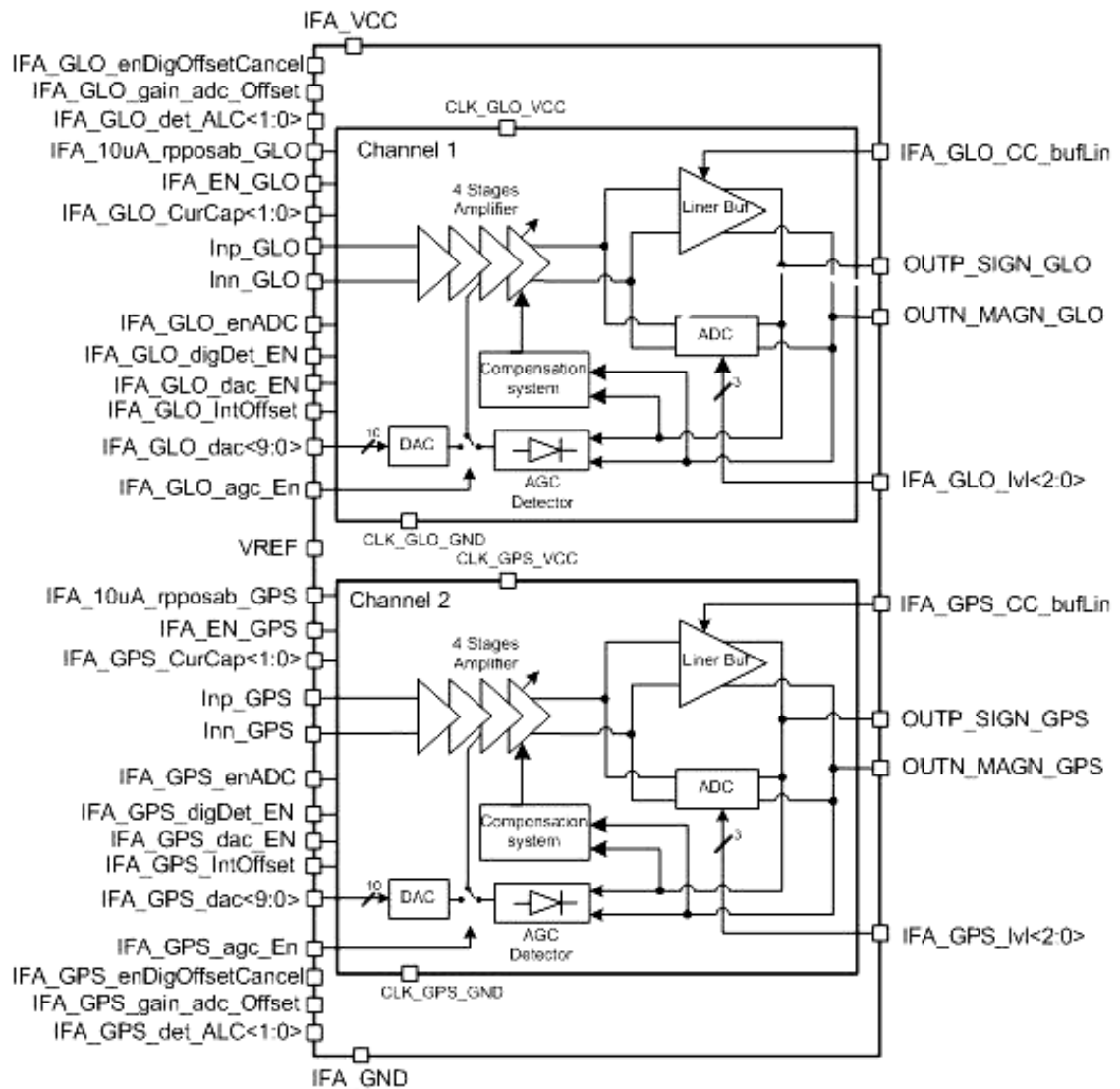


Figure 1: Intermediate frequency amplifier structure

## 5 PIN DESCRIPTION

| Name                                 | Direction | Description   |
|--------------------------------------|-----------|---|
| VREF                                 | I         | Reference voltage                                     |
| IFA_VCC                              | IO        | Supply voltage 1.8 V                                  |
| IFA_GND                              | IO        | Ground  |
| <b>Channel 1 IFA pin description</b> |           |   |
| IFA_10uA_rposab_GLO                  | I         | Reference current (10 uA)                             |
| Inp_GLO                              | I         | Analog differential input                             |
| Inn_GLO                              | I         |   |
| IFA_EN_GLO                           | I         | IFA enable/disable                                    |
| IFA_GLO_enADC                        | I         | ADC mode enable                                       |
| IFA_GLO_agcEN                        | I         | AGC mode enable                                       |
| IFA_GLO_digDet_EN                    | I         | Digital detector enable                               |
| IFA_GLO_dac_EN                       | I         | DAC enable  |
| IFA_GLO_IntOffset                    | I         | DC output voltage offset compensation enable          |
| IFA_GLO_lvl<2:0>                     | I         | ADC comparator level adjustment                       |
| IFA_GLO_dac<9:0>                     | I         | Digital code for IFA gain control or AGC control      |
| IFA_GLO_CurCap<1:0>                  | I         | Speed capability adjustment of digital and analog AGC |
| IFA_GLO_CC_bufLin                    | I         | Linear buffer mode                                    |
| IFA_GLO_enDigOffsetCancel            | I         | Digital DC voltage offset compensation enable         |
| IFA_GLO_gain_adc_Offset              | I         | Offset compensation system adjustment                 |
| IFA_GLO_det_ALC<1:0>                 | I         | AGC level commutation                                 |
| OUTPUT_SIGN_GLO                      | O         | Analog/digital differential output                    |
| OUTPUT_MAGN_GLO                      | O         |   |
| CLK_GLO_VCC                          | IO        | Digital supply voltage                                |
| CLK_GLO_GND                          | IO        | Digital ground  |
| <b>Channel 1 IFA pin description</b> |           |   |
| IFA_10uA_rposab_GPS                  | I         | Reference current (10 uA)                             |
| Inp_GPS                              | I         | Analog differential input                             |
| Inn_GPS                              | I         |   |
| IFA_EN_GPS                           | I         | IFA enable/disable                                    |
| IFA_GPS_enADC                        | I         | ADC mode enable                                       |
| IFA_GPS_agcEN                        | I         | AGC mode enable                                       |
| IFA_GPS_digDet_EN                    | I         | Digital detector enable                               |
| IFA_GPS_dac_EN                       | I         | DAC enable  |
| IFA_GPS_IntOffset                    | I         | DC output voltage offset compensation enable          |
| IFA_GPS_lvl<2:0>                     | I         | ADC comparator level adjustment                       |
| IFA_GPS_dac<9:0>                     | I         | Digital code for IFA gain control or AGC control      |
| IFA_GPS_CurCap<1:0>                  | I         | Speed capability adjustment of digital and analog AGC |
| IFA_GPS_CC_bufLin                    | I         | Linear buffer mode                                    |
| IFA_GPS_enDigOffsetCancel            | I         | Digital DC voltage offset compensation enable         |
| IFA_GPS_gain_adc_Offset              | I         | Offset compensation system adjustment                 |

Table "Pin Description" (continue)

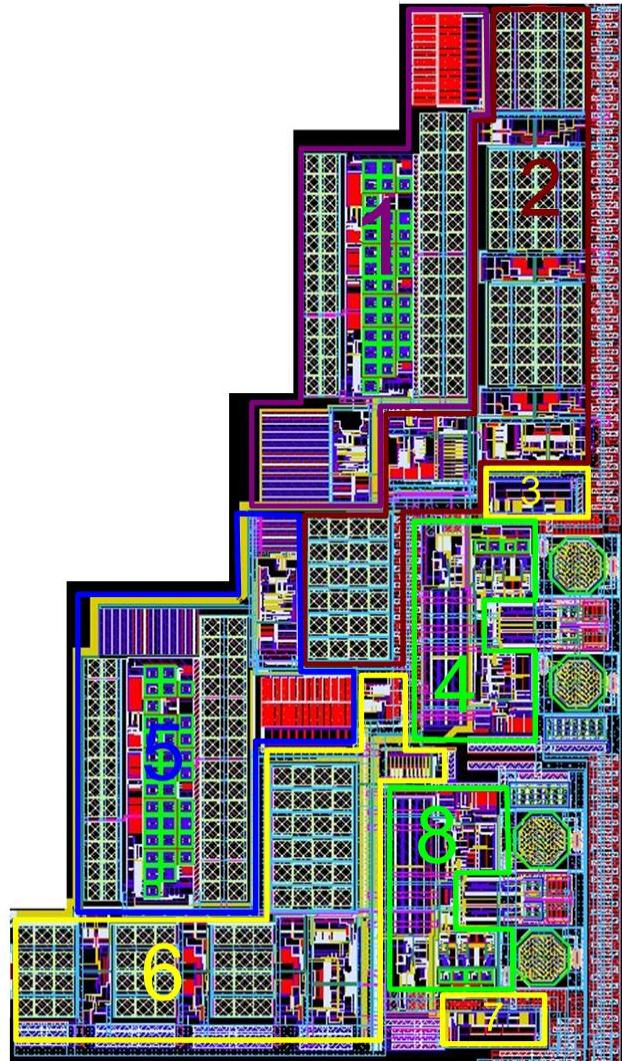
| <b>Name</b>          | <b>Direction</b> | <b>Description</b>                 |
|----------------------|------------------|------------------------------------|
| IFA_GPS_det_ALC<1:0> | I                | AGC level commutation              |
| OUTPUT_SIGN_GPS      | O                | Analog/digital differential output |
| OUTPUT_MAGN_GPS      | O                |                                    |
| CLK_GPS_VCC          | IO               | Digital supply voltage             |
| CLK_GPS_GND          | IO               | Digital ground                     |

## 6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

**Table 1:** Block dimensions

| Dimension | Value | Unit |
|-----------|-------|------|
| Height    | 980   | um   |
| Width     | 1695  | um   |



**Figure 2:** Device layout

1. Detector (Channel 1)
2. IFA core (Channel 1)
3. Linear buffer (Channel 1)
4. ADC (Channel 1)
5. Detector (Channel 2)
6. IFA core (Channel 2)
7. Linear buffer (Channel 2)
8. ADC (Channel 2)

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ SMIC CMOS 0.18 um  
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_ 1.1 mm<sup>2</sup>

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc} = 1.7 \div 1.9$  V and  $T_j = -45 \div +85$  °C. Typical values are at  $V_{cc} = 1.8$  V and  $T_j = +27$  °C, unless otherwise specified.

| Parameter                                | Symbol         | Condition   | Value |      |      | Unit |
|--|----------------|---|-------|------|------|------|
|  |                |   | min   | typ. | max  |      |
| Supply voltage                           | $V_{cc}$       | -   | 1.7   | 1.8  | 1.9  | V    |
| Operating temperature range              | $T_j$          | -   | -45   | 27   | 85   | °C   |
| Frequency range                          | F              | -   | 7     | -    | 20   | MHz  |
| Noise figure                             | NF             | Maximum gain mode   | -     | 6.5  | 9.4  | dB   |
|  |                | 30 dB less than maximum amplification   | -     | 6.8  | 9.8  | dB   |
| Group delay time ripple                  | $t_{del}$      | Bandwidth 7...20 MHz  | -     | 1.8  | -    | ns   |
| Gain                                     | $G_{IFA}$      | -   | 0     | -    | 62   | dB   |
| Input impedance                          | $R_{in}$       | -   | -     | 2    | -    | kOhm |
| Output impedance                         | $R_{out}$      | IFA_GLO_CC_bufLin = "1"   | -     | -    | 260  | Ohm  |
|  |                | IFA_GLO_CC_bufLin = "0"   | -     | -    | 320  |      |
| Peak-to-peak differential output voltage | $A_{in\ p-p}$  | 2pF load, sin signal<br>OUTPUT_SIGN_GLO,<br>OUTPUT_MAGN_GLO –<br>For channel 1;<br>OUTPUT_SIGN_GPS,<br>OUTPUT_MAGN_GPS -<br>For channel 2 | -     | 200  | -    | mV   |
| DC voltage                               | $V_{IFA\_dif}$ | Linear mode: for<br>OUTPUT_SIGN_GLO,<br>OUTPUT_MAGN_GLO –<br>For channel 1;<br>OUTPUT_SIGN_GPS,<br>OUTPUT_MAGN_GPS -<br>For channel 2     | -     | 1.46 | -    | V    |
| ADC resolution                           | K              | -   | -     | 2    | -    | bit  |
| ADC output signal level                  | $V_{dig}$      | Preset 1  | -     | 1.0  | -    | V    |
|  |                | Preset 2  | -     | 1.2  |      |      |
|  |                | Preset 3  | -     | 1.5  |      |      |
|  |                | Preset 4  | -     | 1.8  |      |      |
| Supply current                           | $I_{cc}$       | Linear mode   | -     | 3.1  | 3.7  | mA   |
|  | $I_{dig}$      | Digital mode  | -     | 3    | -    |      |
| Stand-by current                         | $I_{stb}$      | -   | -     | 15   | 1800 | nA   |

Table “Electrical Characteristics” (continue)

| Parameter                                | Symbol        | Condition  | Value         |      |     | Unit |
|--|---------------|--|---------------|------|-----|------|
|  |               |  | min           | typ. | max |      |
| Output logic-level high (digital output) | $V_{OH\_dig}$ | OUTPUT_SIGN_GLO, OUTPUT_MAGN_GLO – For channel 1; OUTPUT_SIGN_GPS, OUTPUT_MAGN_GPS – For channel 2 | $V_{dig}-100$ | -    | -   | mV   |
| Output logic-level low (digital output)  | $V_{OL\_dig}$ | OUTPUT_SIGN_GLO, OUTPUT_MAGN_GLO – For channel 1; OUTPUT_SIGN_GPS, OUTPUT_MAGN_GPS – For channel 2 | -             | -    | 100 | mV   |
| Input logic-level high                   | $V_{IH}$      | For digital inputs   | $0.7V_{cc}$   | -    | 3.6 | V    |
| Input logic-level low                    | $V_{IL}$      |  | -0.25         | -    | 0.3 | V    |

## 8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation