2 to 27 MHz Intermediate frequency amplifier

SPECIFICATION

1 FEATURES

- TSMC SiGe BiCMOS 180 nm
- Wide gain range (0…66 dB)
- Low group delay time ripple vs. frequency and gain
- Analog and digital output modes
- Automatic gain control (AGC) system
- DC offset compensation in each amplifier stage and output buffer
- AGC detector threshold adjustment in the digital mode
- Analog-digital converter to produce digital output signal
- Portable to other technologies (upon request)

2 APPLICATION

- IF signal amplification
- GNSS receiver

3 OVERVIEW

IFA consist of 3-stages amplifier with tunable gain, AGC system, linear output buffer for differential analog output, analog-digital converter for digital output and output level detector. Each stage of the amplifier has differential input and output. Gain is sequentially reduced from the last stage to the first stage for better noise performance in wide gain range.
Output voltage supported by AGC system:

- For sine waveform 200 mV (peak-to-peak)
- For noise signal 480 mV (peak-to-peak)

The block is fabricated on TSMC SiGe BiCMOS 180 nm technology.

4 STRUCTURE

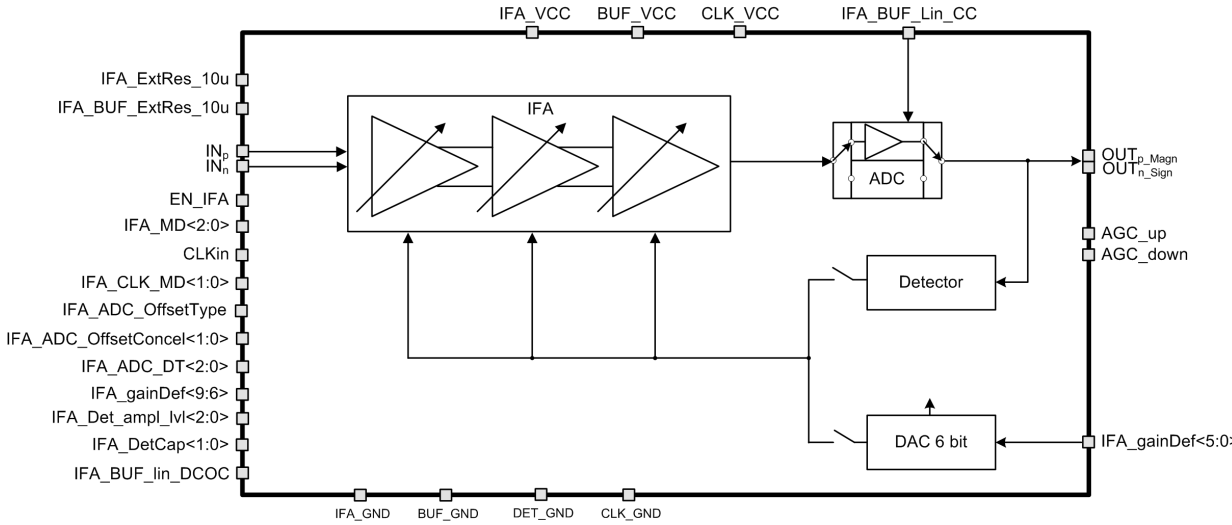

Figure 1: IFA structure

5 PIN DESCRIPTION

Name	Direction	Description
IFA_ExtRes_10u	I	Reference current 10 uA
IFA_BUF_ExtRes_10u	I	Buffer reference current 10 uA
IN_p	I	IFA differential output
IN_n	I	
CLKin	I	Clock input
EN_IFA	I	IFA enable/disable
IFA_MD<2:0>	I	IFA mode
IFA_CLK_MD<1:0>	I	ADC clocking type
IFA_OffsetType	I	Automatic offset compensation type
IFA_ADCOffsetCancel<1:0>	I	Automatic offset compensation system mode
IFA_ADC_DT<2:0>	I	ADC analog detector threshold in digital mode
IFA_gainDef<9:6>	I	IFA gain control in manual mode
IFA_gainDef<5:0>	I	AGS digital detector threshold in digital mode
IFA_Det_ampl_lvl<2:0>	I	Linear AGC system amplitude level
IFA_DetCap<1:0>	I	AGC external capacitor
IFA_BUF_Lin_CC	I	Output buffer current consumption control
IFA_BUF_lin_DCOP	I	IFA output DC operating point
$OUT_{p\ MAGN}$	O	IFA output
$OUT_{n\ SIGN}$	O	
AGC_up	O	Digital detector output for IFA gain adjustment
AGC_down	O	
IFA_VCC	IO	IFA supply voltage 1.8 V
BUF_VCC	IO	Linear buffer supply voltage
CLK_VCC	IO	IFA digital buffer supply voltage
IFA_GND	IO	IFA ground
BUF_GND	IO	Linear buffer ground
DET_GND	IO	IFA detector ground
CLK_GND	IO	IFA digital buffer ground

6 LAYOUT DESCRIPTION

Intermediate-frequency amplifier dimensions are given in the table 1.

Table 1: Block dimension

Dimension	Value	Unit
Height	1170	um
Width	660	um

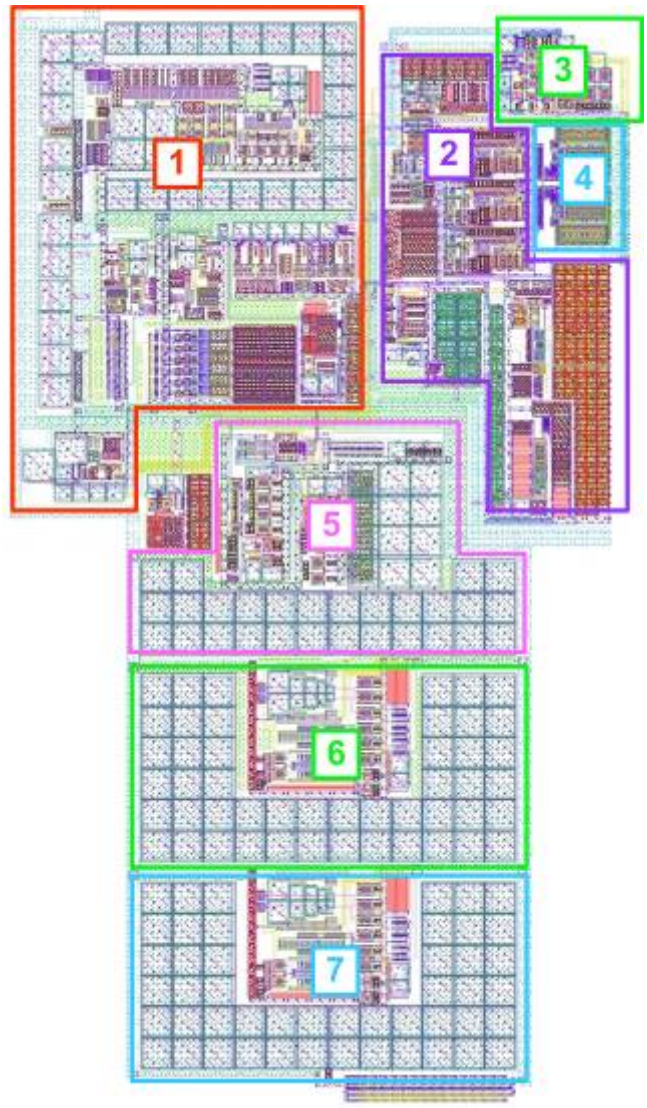

Figure 2: IFA layout

1. Detector
2. ADC
3. Linear buffer
4. Digital buffer
5. IFA 3rd stage
6. IFA 2nd stage
7. IFA 1st stage

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology TSMC SiGe BiCMOS 180 nm
Status silicon proven
Area 0.77 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc_IFA} = 1.6 ÷ 2.0 V and T_j = -45 ÷ +85 °C. Typical values are at V_{cc_IFA} = 1.8 V and T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc_IFA}	-	1.6	1.8	2.0	V
Operating temperature range	T_j	-	-45	27	85	°C
Frequency range	F	-	2	-	27	MHz
Group delay time ripple	t_{del}	From 2 MHz to 27 MHz	-	7.2	11.8	ns
		From 4 MHz to 16 MHz	-	1.7	2.8	
Maximal voltage gain	G_{max}	-	61	66	71	dB
Minimal voltage gain	G_{min}	-	-2.8	-1.0	2.1	dB
Gain control range	ΔG_{IFA}	-	64	67	70	dB
Noise figure	NF	Gain > 30 dB, Rin = 100 Ohm	-	16	19	dB
Input 1dB compression point	P_{1dB}	-	-7.5	-4.0	-	dBm
Amplitude ripple	RP_{AF}	From 2 MHz to 27 MHz	-	0.32	0.52	dB
Peak-to-peak voltage at the differential output	$V_{dif\_p\_p}$	For sine signal	174	198	234	mV
DC operating point	V_{IFA_dif}	-	V_{cc}-0.7	V_{cc}-0.89	V_{cc}-1.07	V
Output logic-level high (digital outputs)	V_{OH_dig}	-	0.7V_{cc}	-	V_{cc}+0.25	V
Output logic-level low (digital outputs)	V_{OL_dig}	-	-0.25	-	0.3V_{cc}	V
ADC capacity	K	-	-	2	-	bit
Current consumption	I_{cc_dif}	-	-	4.0	4.2	mA
	I_{cc_ADC}	F = 20 MHz, Cload 12 pF	-	4.1	5.2	
Stand-by current	I_{stb}	-	-	0.2	7.0	uA
Intput logic-level high	V_{IH}	-	0.7V_{cc}	-	V_{cc}+0.25	V
Intput logic-level low	V_{IL}	-	-0.25	-	0.3V_{cc}	V

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation