

# Intermediate-frequency amplifier

## SPECIFICATION

### 1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Input frequency range from 60 to 83 MHz
- Low noise figure
- High linearity
- Low group delay time ripple and amplitude-frequency characteristic ripple in passband
- Automatic gain control (AGC) system
- AGC detector threshold adjustment in the digital mode
- Linear gain adjustment step ( $< 0.9$  dB)
- Integrated voltage regulators
- Wide temperature range
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

### 2 APPLICATION

- Receivers

### 3 OVERVIEW

IFA consists of 2-stages amplifier, output buffer with tunable gain and two LDO voltage regulators (LDO VR).

Each stage of the amplifier has differential input and output. Gain is sequentially reduced from the buffer to the IFA first stage. Gain is sets by the digital code IFA\_GC<5:0>.

The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

### 4 STRUCTURE

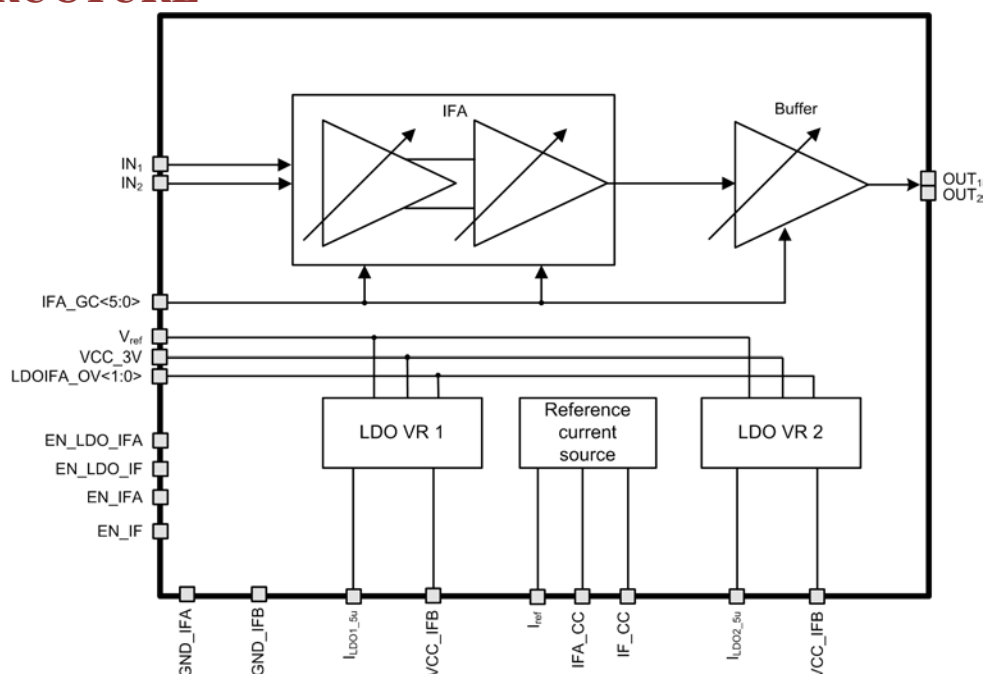


Figure 1: Intermediate-frequency amplifier structure.

## 5 PIN DESCRIPTION

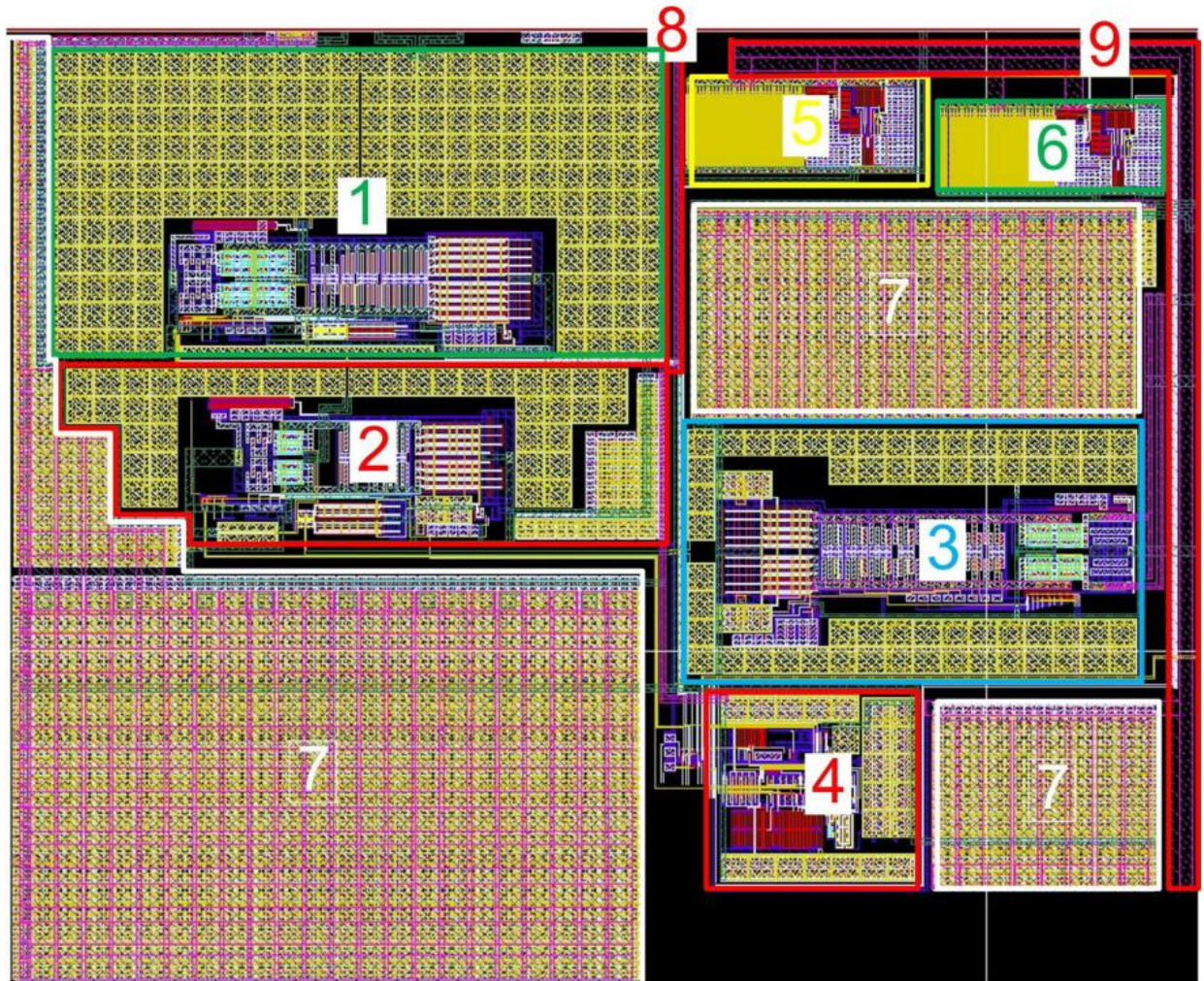
Name	Direction	Description
I <sub>LDO1_5u</sub>	I	LDO VR 1 reference current 5 uA
I <sub>LDO2_5u</sub>	I	LDO VR 2 reference current 5 uA
I <sub>ref</sub>	IO	IFA reference current 10 uA
V <sub>ref</sub>	I	Reference voltage (1.2 V)
IN <sub>1</sub>	I	IFA differential input
IN <sub>2</sub>	I	
EN_LDO_IFA	I	IFA LDO VR enable/disable
EN_LDO_IF	I	IFA buffer LDO VR enable/disable
EN_IFA	I	IFA enable/disable
EN_IF	I	IFA buffer enable/disable
IFA_GC<5:0>	I	IFA gain control
LDOIFA_OV<1:0>	I	IFA stabilized voltage control
IFA_CC	I	IFA current consumption control
IF_CC	I	IFA buffer current consumption control
OUT <sub>1</sub>	O	Differential output
OUT <sub>2</sub>	O	
VCC_3V	IO	3V supply voltage
GND_IFA	IO	IFA ground
GND_IFB	IO	Output buffer ground

## 6 LAYOUT DESCRIPTION

Intermediate-frequency amplifier dimensions are given in the table 1.

**Table 1:** Block dimensions

Dimension	Value	Unit
Height	1130	um
Width	1410	um



**Figure 2:** Intermediate-frequency amplifier layout view

1. IFA 1<sup>st</sup> stage
2. IFA 2<sup>nd</sup> stage
3. IF buffer
4. IFA reference current source
5. IFA LDO VR
6. IFA buffer LDO VR
7. Supply voltage filter capacitors
8. IFA supply voltage
9. 3V supply voltage

## 7 OPERATING CHARACTERISTICS

### 7.1 TECHNICAL CHARACTERISTICS

Technology \_\_\_\_\_ iHP SiGe BiCMOS 0.25  $\mu\text{m}$   
 Status \_\_\_\_\_ silicon proven  
 Area \_\_\_\_\_  $1.6 \text{ mm}^2$

### 7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for  $V_{cc} = 2.9 \div 3.3\text{V}$  and  $T_a = -60 \div +145^\circ\text{C}$ . Typical values are at  $V_{cc} = 3.0\text{V}$ ,  $T_a = +27^\circ\text{C}$ , unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ	max	
Supply voltage	$V_{cc}$	-	2.9	3.0	3.3	V
Operating temperature range	$T_a$	-	-60	27	+125	$^\circ\text{C}$
Frequency range	$F_{IN}$	-	60	-	83	MHz
Gain	G	Maximum	33	37	40	dB
		Minimum	-9	-8	-7.4	
Gain control range	$\Delta G$	-	42	45	-	dB
Gain control step	k	Maximum	-	0.8	0.9	dB
Noise figure	NF	Gain 23 dB	-	8.9	11.5	dB
		Gain 18 dB	-	-	13.3	
Amplitude ripple	$RP_{AF}$	IF band from 61.5 to 82.2 MHz	-	0.3	0.45	dB
Group delay ripple	$t_{del}$	IF band from 61.5 to 82.2 MHz	-	0.3	0.4	ns
Input 1dB compression point	$P_{1dB}$	Gain 23 dB	-16	-15.3	-	dBm
		Gain 18 dB	-11	-10.7	-	
Input resistance	$R_{IN}$	At a differential input	-	50	-	$\Omega$
Output resistance	$R_{OUT}$	At a differential input	-	200	-	$\Omega$
Reference voltage	$V_{ref}$	-	-	1.2	-	V
Supply current	$I_{cc}$	-	-	34.7	41	mA
Stand-by current	$I_{stb}$	-	-	0.04	3.1	$\mu\text{A}$
Input logic-level high	$V_{IH}$	For digital inputs	$0.7 V_{cc}$	-	$V_{cc}+0.25$	V
Input logic-level low	$V_{IL}$		-0.25	-	0.3	V

## 8 DELIVERABLES

IP contents:

- Schematic or NetList
- Layout or blackbox
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

## REVISION HISTORY

From version 1.1:

- Subsection 7.2 update