

Intermediate-frequency amplifier

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Input frequency range from 60 to 83 MHz
- Low noise figure
- High linearity
- Low group delay time ripple and amplitude-frequency characteristic ripple in passband
- Automatic gain control (AGC) system
- AGC detector threshold adjustment in the digital mode
- Linear gain adjustment step (< 0.9 dB)
- Integrated voltage regulators
- Wide temperature range
- Portable to other technologies (upon request)

2 APPLICATION

- Receivers

3 OVERVIEW

IFA consists of 2-stages amplifier, output buffer with tunable gain and two LDO voltage regulators (LDO VR).

Each stage of the amplifier has differential input and output. Gain is sequentially reduced from the buffer to the IFA first stage. Gain is sets by the digital code IFA_GC<5:0>.

The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

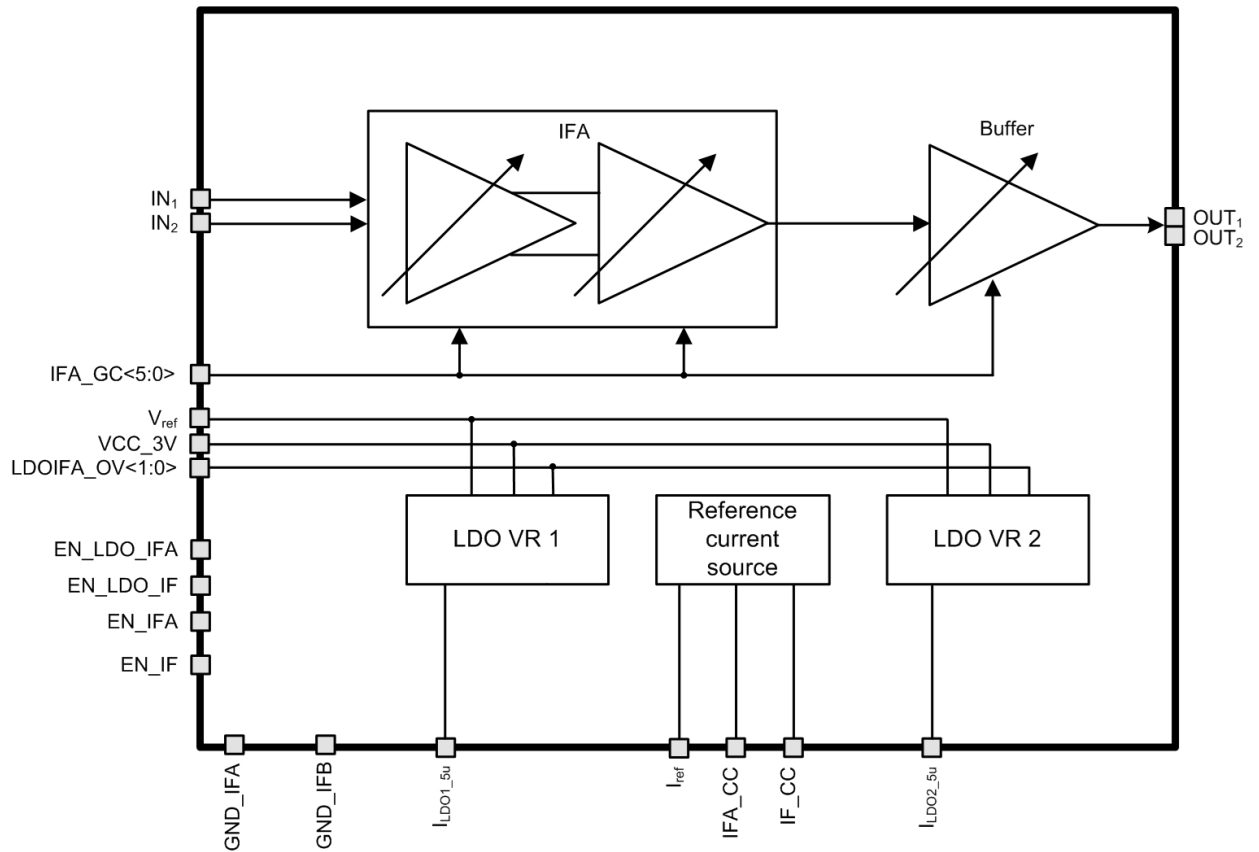


Figure 1: Intermediate-frequency amplifier structure

PIN DESCRIPTION

| Name | Direction | Description |
|----------------------|------------------|--|
| I _{LDO1_5u} | I | LDO VR 1 reference current 5 uA |
| I _{LDO2_5u} | I | LDO VR 2 reference current 5 uA |
| I _{ref} | IO | IFA reference current 10 uA |
| V _{ref} | I | Reference voltage (1.2 V) |
| IN ₁ | I | IFA differential input |
| IN ₂ | I | |
| EN_LDO_IFA | I | IFA LDO VR enable/disable |
| EN_LDO_IF | I | IFA buffer LDO VR enable/disable |
| EN_IFA | I | IFA enable/disable |
| EN_IF | I | IFA buffer enable/disable |
| IFA_GC<5:0> | I | IFA gain control |
| LDOIFA_OV<1:0> | I | IFA stabilized voltage control |
| IFA_CC | I | IFA current consumption control |
| IF_CC | I | IFA buffer current consumption control |
| OUT ₁ | O | Differential output |
| OUT ₂ | O | |
| VCC_3V | IO | supply voltage 3 V |
| GND_IFA | IO | IFA ground |
| GND_IFB | IO | Output buffer ground |

5 LAYOUT DESCRIPTION

Intermediate-frequency amplifier dimensions are given in the table 1.

Table 1: Block dimensions

| Dimension | Value | Unit |
|-----------|-------|------|
| Height | 1130 | um |
| Width | 1410 | um |

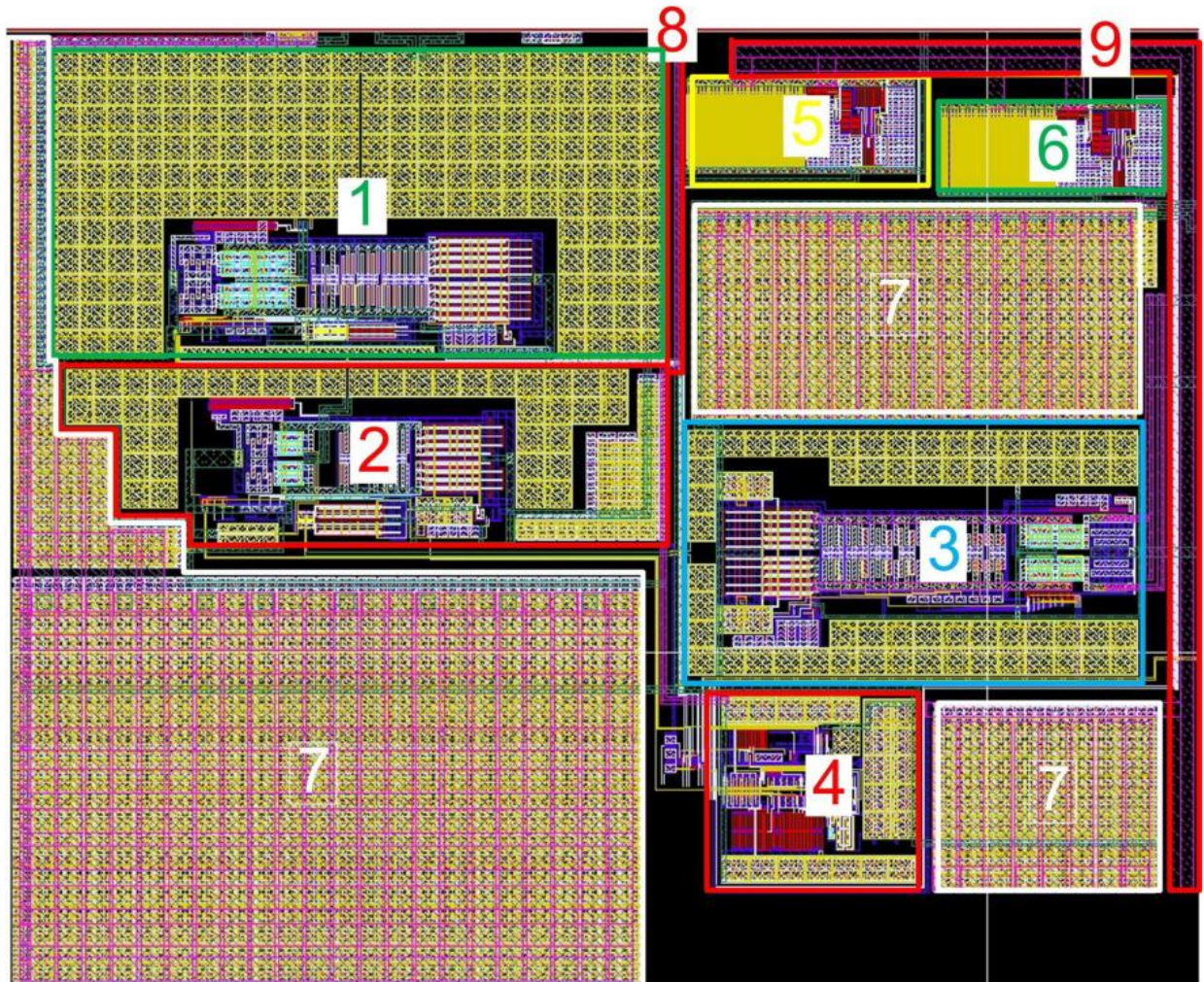


Figure 2: Intermediate-frequency amplifier layout

1. IFA 1st stage
2. IFA 2nd stage
3. IF buffer
4. IFA reference current source
5. IFA LDO VR
6. IFA buffer LDO VR
7. Supply voltage filter capacitors
8. IFA supply voltage
9. Supply voltage 3 V

6 OPERATING CHARACTERISTICS

6.1 TECHNICAL CHARACTERISTICS

Technology _____ iHP SiGe BiCMOS 0.25 um
 Status _____ silicon proven
 Area _____ 1.6 mm²

6.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{cc} = 2.9 \div 3.3$ V and $T_j = -60 \div +145$ °C. Typical values are at $V_{cc} = 3.0$ V, $T_j = +27$ °C, unless otherwise specified.

| Parameter | Symbol | Condition | Value | | | Unit |
|-----------------------------|------------|-------------------------------|-------------|-------|---------------|------|
| | | | min | typ. | max | |
| Supply voltage | V_{cc} | - | 2.9 | 3.0 | 3.3 | V |
| Operating temperature range | T_j | - | -60 | 27 | +125 | °C |
| Frequency range | F_{IN} | - | 60 | - | 83 | MHz |
| Gain | G | Maximum | 33 | 37 | 40 | dB |
| | | Minimum | -9 | -8 | -7.4 | |
| Gain control range | ΔG | - | 42 | 45 | - | dB |
| Gain control step | k | Maximum | - | 0.8 | 0.9 | dB |
| Noise figure | NF | Gain 23 dB | - | 8.9 | 11.5 | dB |
| | | Gain 18 dB | - | - | 13.3 | |
| Amplitude ripple | RP_{AF} | IF band from 61.5 to 82.2 MHz | - | 0.3 | 0.45 | dB |
| Group delay ripple | t_{del} | IF band from 61.5 to 82.2 MHz | - | 0.3 | 0.4 | ns |
| Input 1dB compression point | P_{1dB} | Gain 23 dB | -16 | -15.3 | - | dBm |
| | | Gain 18 dB | -11 | -10.7 | - | |
| Input resistance | R_{IN} | At a differential input | - | 50 | - | Ohm |
| Output resistance | R_{OUT} | At a differential input | - | 200 | - | Ohm |
| Reference voltage | V_{ref} | - | - | 1.2 | - | V |
| Supply current | I_{cc} | - | - | 34.7 | 41 | mA |
| Stand-by current | I_{stb} | - | - | 0.04 | 3.1 | uA |
| Input logic-level high | V_{IH} | For digital inputs | $0.7V_{cc}$ | - | $V_{cc}+0.25$ | V |
| Input logic-level low | V_{IL} | | -0.25 | - | 0.3 | V |

7 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.1:

- Subsection 7.2 update