Intermediate-frequency amplifier

SPECIFICATION

1 FEATURES

- iHP SiGe BiCMOS 0.25 um
- Wide gain range from 0 to 43 dB
- Tunable bandwidth from 8 to 512 kHz
- Output offset voltage digital setting more than +/- 50 mV
- Input offset voltage analog compensation in the range -50…+ 50 mV
- Input impedance 20 kOhm
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, AMS, Vanguard, SilTerra

2 APPLICATION

- Wide-band receiver

3 OVERVIEW

The device is a two channel intermediate-frequency amplifier (IFA). Each channel consists of 1 stage amplifier with differential inputs/outputs, programmable gain and offset voltage setting. Input/output tuning capacitors with IFA input/output impedance create 2^{nd} order LPF. Signal reception mode with 8 kHz bandwidth requires external 2 nF capacitor. Analog compensation system is used to reduce IFA output offset voltage. There is an option of voltage reference levels former for ADC.
The block is fabricated on iHP SiGe BiCMOS 0.25 um technology.

4 STRUCTURE

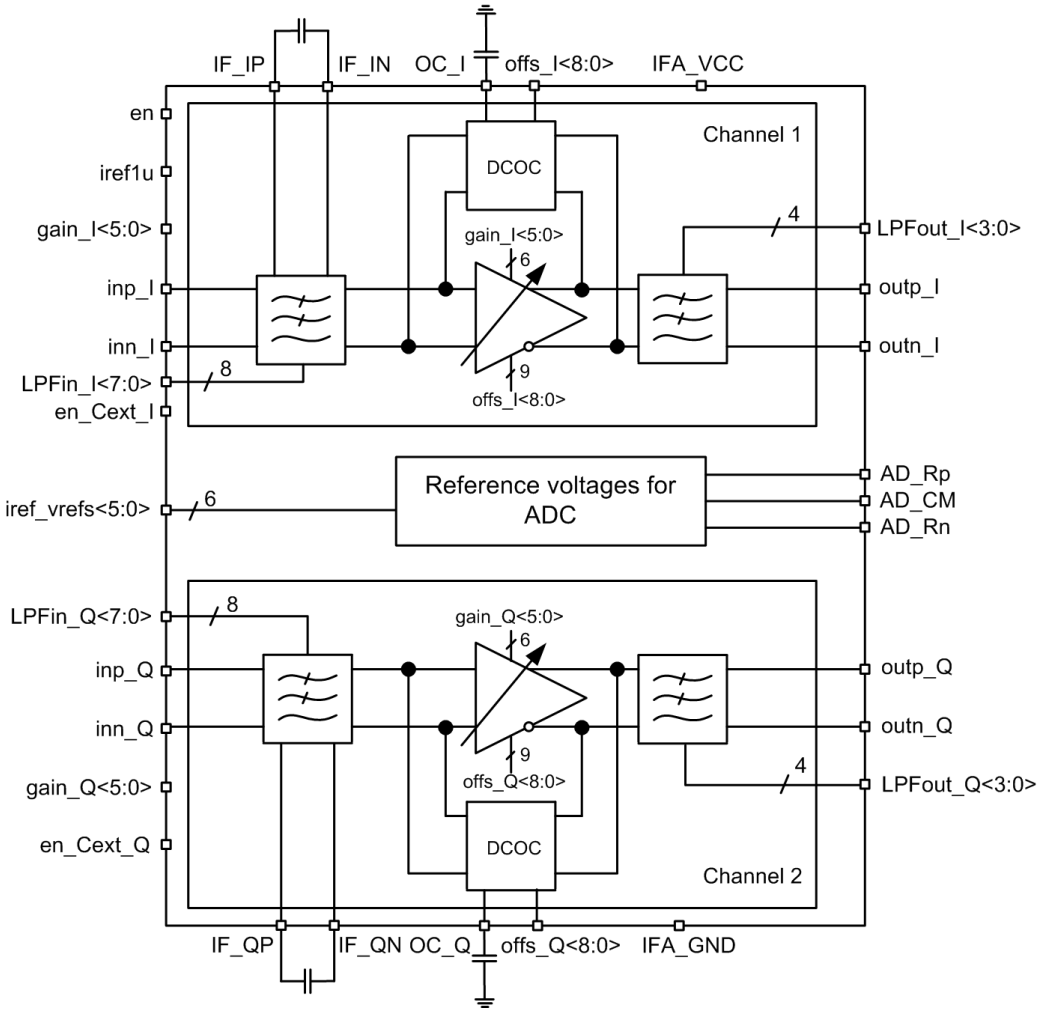

Figure 1: Intermediate-frequency amplifier structure

5 PIN DESCRIPTION

Name	Direction	Description
iref1u	I	Reference current (1 uA)
iref_vrefs<5:0>	I	ADC reference voltage current control
en	I	Enable/disable
AD_Rp	IO	ADC comparators high level reference voltage (1.3 V)
AD_CM	IO	ADC comparators middle level reference voltage (0.9 V)
AD_Rn	IO	ADC comparators low level reference voltage (0.5 V)
IFA_VCC	IO	Supply voltage 1.8 V
IFA_GND	IO	Ground
Channel 1 IFA pin description		
inp_I	I	Analog differential input
inn_I	I	
offs_I<8:0>	I	Output voltage DC offset control
gain_I<5:0>	I	IFA gain control
LPFin_I<7:0>	I	Input tuned capacitors control
LPFout_I<3:0>	I	Output tuned capacitors control
en_Cext_I	I	External input capacitors control
outp_I	O	Analog differential output
outn_I	O	
OC_I	IO	External integrated capacitor connection
IF_IP	IO	External capacitor connection
IF_IN	IO	
Channel 2 IFA pin description		
inp_Q	I	Analog differential input
inn_Q	I	
offs_Q<8:0>	I	Output voltage DC offset control
gain_Q<5:0>	I	IFA gain control
LPFin_Q<7:0>	I	Input tuned capacitors control
LPFout_Q<3:0>	I	Output tuned capacitors control
en_Cext_Q	I	External input capacitors control
outp_Q	O	Analog differential output
outn_Q	O	
OC_Q	IO	External integrated capacitor connection
IF_QP	IO	External capacitor connection
IF_QN	IO	

6 LAYOUT DESCRIPTION

The block dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	1290	um
Width	1800	um

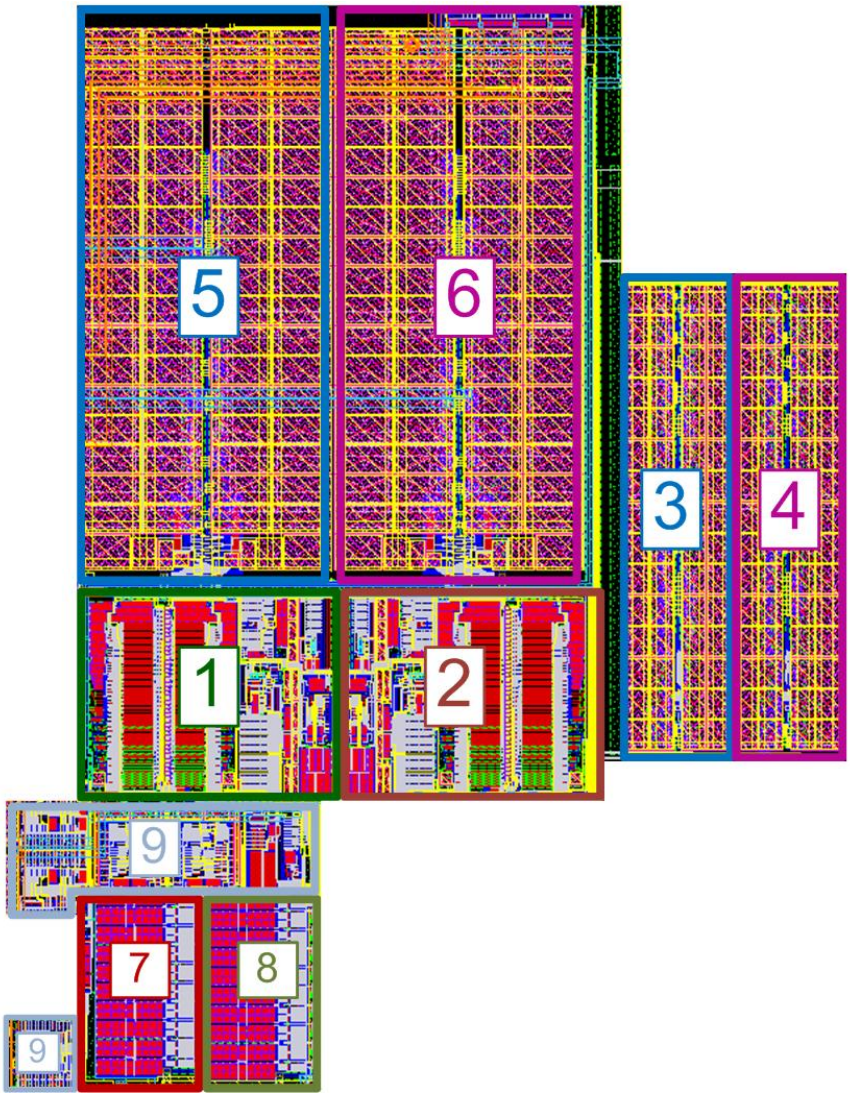

Figure 2: Device layout

1. IFA core (channel 1)
2. IFA core (channel 2)
3. Output LPF (channel 1)
4. Output LPF (channel 2)
5. Input LPF (channel 1)
6. Input LPF (channel 2)
7. DAC (channel 1)
8. DAC (channel 2)
9. Block of reference voltages for ADC

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology iHP SiGe BiCMOS 0.25 um
Status silicon proven
Area 1.72mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for V_{cc} = 1.7 ÷ 1.9 V and T_j = -45 ÷ +85 °C. Typical values are at V_{cc} = 1.8 V and T_j = +27 °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc}	-	1.7	1.8	1.9	V
Operating temperature range	T_j	-	-45	27	85	ºC
Frequency range	F	-	8	-	800	kHz
Tunable bandwidth	F_t	-	8	-	512	kHz
Gain range	G	-	-0.27	-	43	dB
Noise figure	NF	G = 0, F = 10 kHz	-	11.85	-	dB
		G = 43 dB	-	5.516	-	
Intermodulation immunity	IM3	P_{in}=-28.5 dBm	-	-75	-	dB
Input 1dB compression point	P_{1dB}	-	-	-2.7	-	dBm
Input impedance	R_{in}	-	-	20	-	kOhm
Input offset voltage range	V_{off}	Analog compensation	-50	-	50	mV
		Digital setting	-50	-	50	
Current consumption	I_{cc}	Preset 1	-	2.06	-	mA
		Preset 2	-	1.55	-	
		Preset 3	-	1.27	-	
		Preset 4	-	1.11	-	
		Preset 5	-	1.00	-	
Input logic-level high	V_{IH}	For digital inputs	0.7 V_{cc}	-	V_{cc}+0.25	V
Input logic-level low	V_{IL}		-0.25	-	0.3 V_{cc}	V

Table 2: Preset description

Preset	Bandwidth mode	LPFin<7:0> control signal	LPFout<3:0> control signal	External capacitor connection en_Cext	iref_vrefs<5:0> control signal
Preset 1	8 kHz	180	13	yes	1
Preset 2	64 kHz	190	7	no	4
Preset 3	128 kHz	87	4	no	9
Preset 4	256 kHz	41	1	no	19
Preset 5	512 kHz	16	0	no	39

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation

REVISION HISTORY

From version 1.1:

- Subsection 7.2 update