Intermediate-frequency amplifier

SPECIFICATION

1 FEATURES

- AMS BiCMOS 0.35 um
- Wide gain range (0…64 dB)
- Low group delay time ripple vs. frequency and gain
- Analog and digital output modes
- Automatic gain control (AGC) system
- AGC detector threshold adjustment in the digital mode
- Supported foundries: TSMC, UMC, Global Foundries, SMIC, iHP, AMS, Vanguard, SilTerra

2 APPLICATION

- Receivers

3 OVERVIEW

IFA consists of 3-stages amplifier with tunable gain, AGC system, linear output buffer for differential analog output, analog-digital converter for 1.5-bits digital output.
Each stage of the amplifier has differential input and output. Gain is sequentially reduced from the last stage to the first stage. Also gain can be fixed by the digital code DAC<9:0>.
The block is fabricated on AMS BiCMOS 0.35 um technology.

4 STRUCTURE

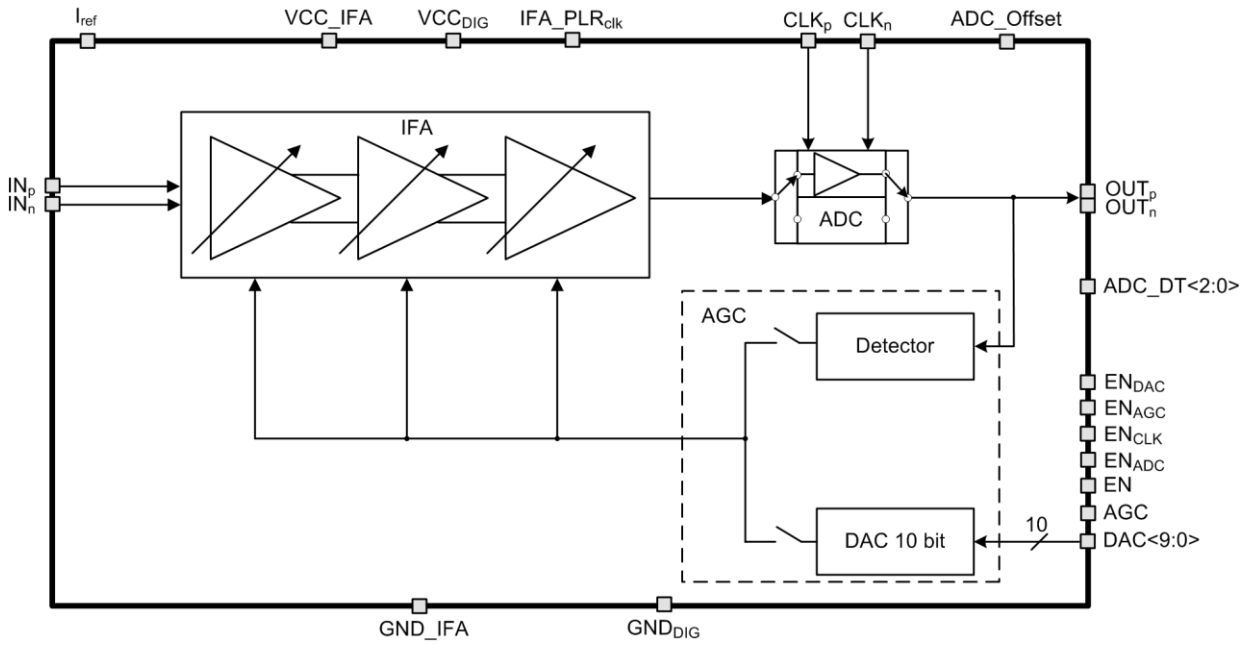

Figure 1: Intermediate-frequency amplifier structure

5 PIN DESCRIPTION

Name	Direction	Description
I_{ref}	I	Reference current 10 uA
IN_p	I	Differential input
IN_n	I	
CLK_p	I	Differential clock input
CLK_n	I	
ADC_Offset	I	DC offset compensation mode: IFA buffer/ADC output-referred or IFA buffer/ADC input-referred
ADC_DT<2:0>	I	Digital code defined ADC analog detector threshold
DAC<9:0>	I	Digital code for DAC
IFA_PLR_{clk}	I	IFA clock frequency polarity
EN_{DAC}	I	IFA AGC mode
EN_{AGC}	I	
EN_{ADC}	I	IFA output type (differential linear/digital CMOS)
EN_{CLK}	I	IFA digital outputs clocking enable/disable
EN	I	IFA enable/disable
AGC	IO	External capacitor for AGC
OUT_p	O	Differential/digital output
OUT_n	O	
VCC_IFA	IO	IFA supply voltage 3.15 V
VCC_{DIG}	IO	Digital buffer supply voltage 3.15 V
GND_IFA	IO	IFA ground
GND_{DIG}	IO	Digital buffer ground

6 LAYOUT DESCRIPTION

Intermediate-frequency amplifier dimensions are given in the table 1.

Table 1: Block dimensions

Dimension	Value	Unit
Height	1170	um
Width	890	um

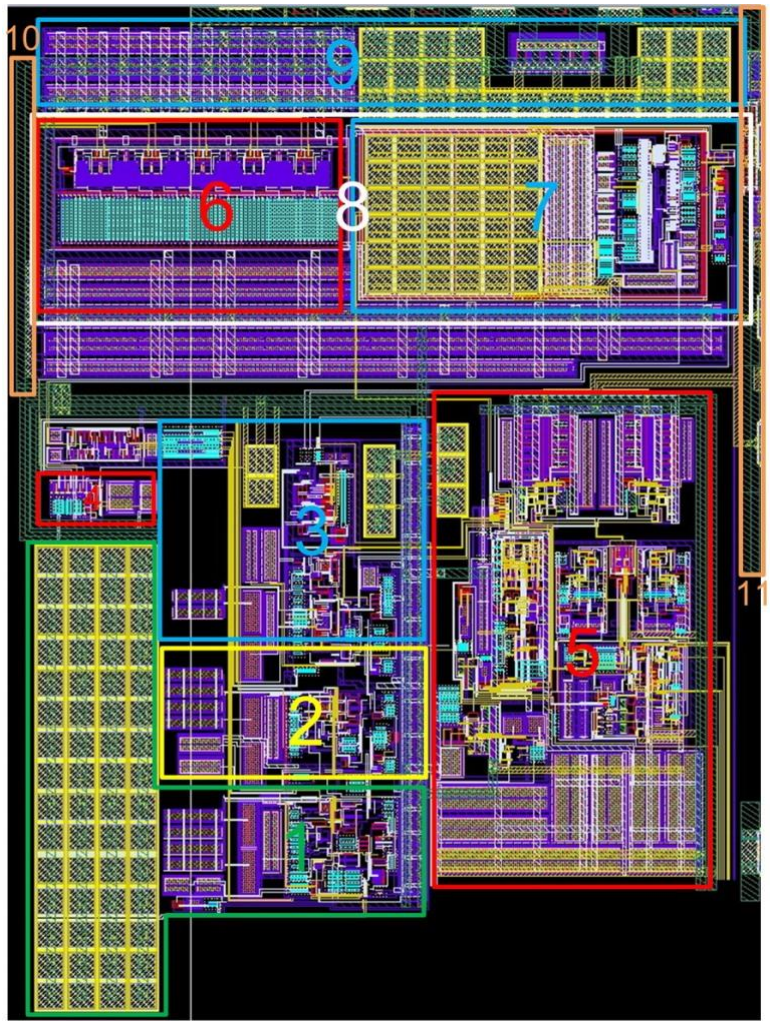

Figure 2: Intermediate-frequency amplifier layout

1. IFA 1st stage
2. IFA 2nd stage
3. IFA 3rd stage
4. IFA reference current source
5. Linear and digital buffer with ADC
6. Detector
7. 10 bit DAC
8. AGC system
9. Filter capacitors
10. Supply voltage bus
11. Ground bus

7 OPERATING CHARACTERISTICS

7.1 TECHNICAL CHARACTERISTICS

Technology AMS BiCMOS 0.35 um
Status silicon proven
Area 1.04 mm^2

7.2 ELECTRICAL CHARACTERISTICS

The values of electrical characteristics are specified for $V_{cc\_IFA} = V_{cc\_DIG} = 2.8 \div 3.6$ V и $T_j = -40 \div +85$ °C. Typical values are at $V_{cc\_IFA} = V_{cc\_DIG} = 3.15$ V, $T_j = +27$ °C, unless otherwise specified.

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	V_{cc_IFA}	-	2.8	3.15	3.6	V
	V_{cc_DIG}	-	2.8	3.15	3.6	
Operating temperature range	T_j	-	-40	+27	+85	°C
Frequency range	F_{IN}	-	2.5	-	22.5	MHz
Group delay time ripple	t_{del}	From 2.5 MHz to 22.5 MHz	-	1.0	1.4	ns
Maximum gain	G_{MAX}	-	64	75	83	dB
Input impedance	R	-	-	100	-	Ohm
Output impedance	R_{out}	-	-	190	-	Ohm
Noise figure	NF	Maximum gain (input resistanse 100 Ohm)	-	13.4	-	dB
Peak-to-peak voltage at the differential output	$V_{dif\_p\_p}$	Differential load 200 Ohm	170	198*	227	mV
DC operating point	V_{IFA_dif}	For outputs OUT_p, $OUT_{n/}$, linear mode	-	V_{cc_BUF}-1.15	-	V
Output logic-level low (digital outputs)	V_{OH_dig}	For outputs OUT_p, OUT_n, ADC mode. Load current 2 mA	V_{cc_BUF}-0.5	V_{cc_BUF}-0.2	V_{cc}	V
Output logic-level high (digital outputs)	V_{OL_dig}	For outputs OUT_p, OUT_n, ADC mode. Load current 2 mA	0	0.04	0.2	V
ADC resolution	R_{ADC}	-	-	1.5	-	bit
Supply current	I_{cc_dif}	Linear mode	-	4.25	5.2	mA
	I_{cc_ADC}	ADC mode, 20 MHz	-	3.7	-	
Stand-by current	I_{stb}	-	-	0.01	0.1	uA
Input logic-level high	V_{IH}	For digital inputs ADC_Offset, DAC<9:0>, EN_{AGC}, EN_{DAC}	0.7V_{cc_IFA}	-	V_{cc_IFA}+0.25	V
		For digital inputs ADC_DT<2:0>, IFA_PLR_{clk}, EN_{CLK}, EN, EN_{ADC}	0.7V_{cc_BUF}	-	V_{cc_BUF}+0.25	
Input logic-level low	V_{IL}	For digital inputs	-0.25	-	0.3	V

Note:
* – for sinusoidal signal.

8 DELIVERABLES

Depending on license type IP may include:

- Schematic or NetList
- Abstract view (.lef and .lib files)
- Layout (optional)
- Verilog behavior model
- Extracted view (optional)
- GDSII
- DRC, LVS, antenna report
- Test bench with saved configurations (optional)
- Documentation