

## 1 to 30 MHz Intermediate-Frequency Amplifier with Wide Gain Range

### OVERVIEW

IFA consists of 3 stages amplifier with tunable gain, AGC system, linear buffer for analog output and an analog-digital converter (ADC) for 2-bits digital output and a detector of output level.

The amplifier has differential inputs and outputs. Gain is sequentially reduced from the last stage to the first stage. This method allows to keep a low noise figure in wide gain range.

In the analog output mode the circuit controls the gain so that the magnitude of the differential output signal. The signal level is set through `Det_ampl_lvl<2:0>`.

Digital output with AGC for analog signal mode operates similarly to the previous mode.

AGC operates in an automatic control mode of digital detector threshold for digital signal (MAGN).

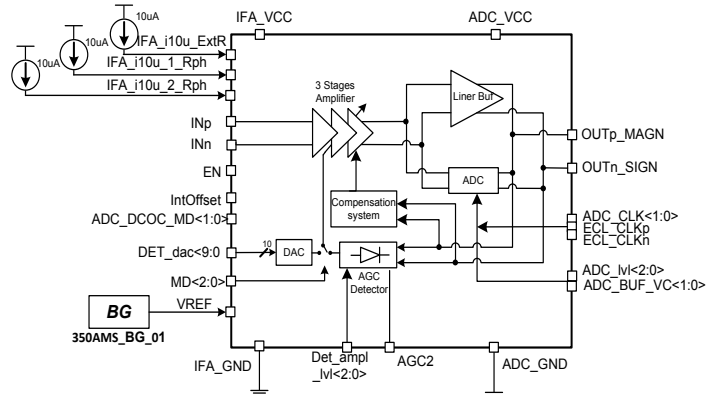
Threshold and gain are set by the DAC code. Digital output level is set 1.8V, 2.4V, 2.7V, `ADC_VCC`.

DC offset compensation system operates both at an amplifier output signal and at a buffer output signal.

IP technology: AMS S35D4M5.

IP status: silicon proven.

Total area: 1.2 mm<sup>2</sup>.



### ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Value			Unit
			min	typ.	max	
Supply voltage	$V_{cc}$ IFA	-	2.85	3.0	3.15	V
	$V_{cc}$ BUF	-	1.8	3.0	3.15	
Operating temperature range	T	-	-60	27	+85	°C
Frequency range	$F_{IN}$	-	1	-	30	MHz
Noise figure	NF	$G = G_{min} + 30dB$ , $v_{rt} 100\Omega$	-	16	19	dB
Input compression point	ICP	$G = G_{min}$	0.5	2	-	dB
Transmission gain	G	max	64	76	-	dB
Gain control range	dG	-	66	79	-	dB
Ripple	$A_{rip}$	Analog output; From 1 MHz to 25 MHz	-	0.5	0.7	dB
Group delay time ripple	GDR	From 2.5 MHz to 18.5 MHz	-	2.2	3	ns
		From 4.5 MHz to 22.5 MHz	-	0.75	1.1	
Peak-to-peak voltage at the differential output	$V_{out}$	For sinusoidal signal	168	198	236	mVp-p
DC voltage	$V_{DC}$	-	$V_{cc}-1.35$	$V_{cc}-1.32$	$V_{cc}-1.3$	V
Supply current	$I_{cc}$	Analog output $R_{out}=200\Omega$	-	4.17	5.37	mA
		Digital output; $C_{load} = 12$ pF	-	6.4	7	
Standby current	$I_{stb}$	-	-	0.2	7	uA
Input logic-high level	$V_{IH}$	For digital inputs	$0.7V_{cc}$	-	$V_{cc}+0.3$	V
Input logic-low level	$V_{IL}$		-	-	$0.3V_{cc}$	V